

# Multi-Valued Logic Device Technology; Overview, Status, and Its Future for Peta-Scale Information Density

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## ABSTRACT

Complementary metal-oxide-semiconductor (CMOS) technology is now facing a power scaling limit to increase integration density. Since 1970s, multi-valued logic (MVL) has been considered as promising alternative to resolve power scaling challenge for increasing information density up to peta-scale level by reducing the system complexity. Over the past several decades, however, a power-scalable and mass-producible MVL technology has been absent so that MVL circuit and system implementation have been delayed. Recently, compact MVL device researches incorporating multiple-switching characteristics in a single device such as 2D heterojunction-based negative-differential resistance (NDR)/transconductance (NDT) devices and quantum-dot/superlattices-based constant intermediate current have been actively performed. Meanwhile, wafer-scale, energy-efficient and variation-tolerant ternary-CMOS (*T*-CMOS) technology has been demonstrated through commercial foundry. In this review paper, an overview for MVL development history including recent studies will be presented. Then, the status and its future research direction of MVL technology will be discussed focusing on the *T*-CMOS technology for peta-scale information processing in semiconductor chip.

## KEY WORDS

Multi-valued logic (MVL), peta-scale, power-scaling limit, ternary-CMOS (*T*-CMOS) technology.

## 1. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) technology has provided the unique economic efficiency to the semiconductor industry by its own geometrical scalability [1]. To achieve the peta-scale information densities ( $\sim 10^{14}/\text{cm}^2$ ), however, the binary Boltzmann switch of CMOS that controls current with potential barrier, face power density limits to giga-scale level ( $\sim 10^9/\text{cm}^2$ ) [2]. This needs for new technology that can overcome the power

density limits is “cycle” of paradigm change since we already experienced these changes from vacuum tubes to the first solid-state bipolar junction transistors (BJTs) in the 1950s, and BJTs to MOS field-effect transistors (MOSFETs) in the 1970s.

Multi-valued logic (MVL) has been considered as one of the promising alternatives since, in principle, the radix ( $R$ ) increase of  $\{0,1,2,\dots\}$  from binary value  $\{0,1\}$  enables the significant increases in information density ( $N=R^d$ ) for the same digit ( $d$ ) and/or reduction of the number of digit ( $d=\log_R N$ ) for the same  $N$ .

Especially, the most efficient way to overcome these power scaling challenges, is to move from a binary to a ternary system, where the system complexity is reduced to  $C = \log_3 N / \log_2 N \approx 63.1\%$  [3][4].

The human brain is an example of an energy-efficient system that uses ternary synaptic weights [5], consuming only  $\sim 20$  W with peta-scale connection densities [6]. The evidences of these brain-inspired systems have been demonstrated by wafer-scale deep-learning (DL) engine with peta-scale memory and fabric bandwidth [7] and ternary-based neural network accelerator with many-core processing-in-memory (PIM) architecture [8] based on binary CMOS technology. Therefore, it can be expected that energy-efficient ternary logic scheme and its stable integration technology enable compact chip-scale DL engines with peta-scale processing capacity.

In practical aspects to integrate ternary system on semiconductor chip, however, there has been no power-scalable and mass-producible basic building block technology for the standard ternary inverter (STI) operation, while positive ternary inverter (PTI) or negative ternary inverter (NTI) can be easily implemented by shifting the transition region of binary CMOS inverter close to  $V_{DD}$  or 0 (GND), respectively. As shown in Figure 1, even though its circuit symbol looks simple and conceptually similar with binary CMOS case, the various ternary device and circuit approaches have been studied over the past few decades. In this review paper, an overview of MVL technologies is presented with a systematic benchmarking of various studies. Then, we present the status and contributions of ternary-CMOS (*T*-CMOS) technology. Finally, the future research direction of MVL technology will be discussed.

## 2. OVERVIEW OF MVL TECHNOLOGIES

In the early stage of MVL technology, ternary logic research to realize STI function has been performed

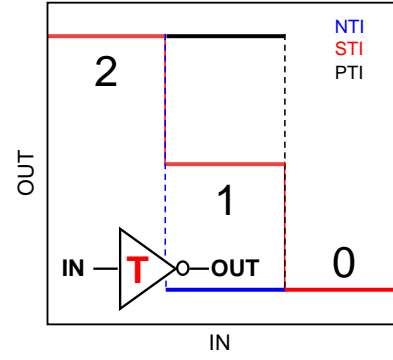


Figure 1. Standard ternary inverter (STI) IN-OUT voltage transfer characteristics with negative (NTI) and positive ternary inverter (PTI). Inset show the circuit symbol of STI building block.

based on CMOS technology owing to its convenience of implementation, but these circuit-level approaches needed additional voltage sources for three voltage states such as  $+V_{DD}/-V_{DD}$  and additional circuit elements for the intermediate states by voltage dividing of  $V_{DD}$  such as two more resistors [9],  $V_{DD}/2$  source with a resistor [10], and with an active load of the depletion/enhancement CMOS in output node [11].

Evidently, those additional circuit components lead to an increase in the number of devices (4-6) more than the ternary states ( $R=3$ ) even in a basic building block of STI configuration. For the area efficiency, carbon nanotube (CNT) FETs [12], [13] and single-electron transistors (SETs) [14] tried to replace CMOS components in those circuit-level approaches. Thus, it is the key challenge that the controllability of 1D CNT diameters and 0D quantum-dot size variations should be guaranteed in very-large-scale integration (VLSI). Recent advancement of a large-scale CNTFET integration [15] opens a new chance for the realization of CNT-based MVL technology. Furthermore, the stacked interfacial devices that can be processed by low thermal processes such as a graphene barrister

Table 1. Benchmarking result of the recent MVL device technologies

Scheme	Multi-threshold									Single-threshold
Device Char.	Step <i>I-V</i> (constant on-current)		NDR	NDT (multiple on-off switching)						Step <i>I-V</i> w. off-current
Reference	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]
Physical principle	Coulomb blockade	Quantized mobility edge	BTBT* (broken-gap)	multi-Dirac voltage	Non-uniform bandgap	Reverse saturated junction	Anti-ambipolar transistor (inverted ambipolar transfer)	G-potential control	BTBT* (Zener diode)	
Device	QDG FET	ZnO composite nanolayer	Hetero-junction	Graphene (G)FET	Hetero-junction (H)FET	UTB** p-i-n FET	Organic HJFETs	HJFET	MOSFET	
Material	Silicon QD in SiO <sub>2</sub>	ZnO /Organic	BP /ReS <sub>2</sub>	G/Pt (n) G/Al (p)	BP /MoS <sub>2</sub>	Silicon	$\alpha$ -6T /PTCDI-C8	DNTT /PTCDI-C13	WS <sub>2</sub> G /WSe <sub>2</sub>	Silicon
Load	p-QDG FET	Resistor	BP p-channel TFT	p-GFET	BP FET	Resistor	PTCDI-C8 n-transistor	PTCDI-C13	p-FET (model)	CMOS
$V_{DD}$ (V)	0.6 (Sim.)	5	2	2	2	Pulse 0.5 - 0.625	10	50	2.1 (Sim.)	0.5/0.7/1

\*BTBT: band-to-band tunneling; \*\*UTB: ultra-thin body

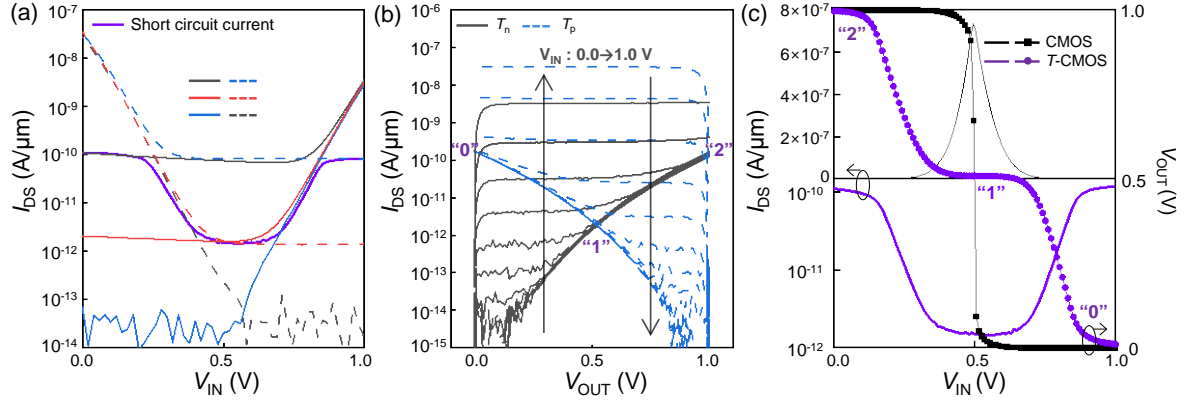


Figure 2. The off-state working  $T$ -CMOS characteristics: (a) transfer  $I_{DS}$ - $V_{IN}$  for  $|V_{DS}| = 0.1, 0.5, 1.0$  V and (b) output  $I_{DS}$ - $V_{OUT}$  for varying  $V_{IN}$  from 0 V to 1 V (step: 0.1 V) with high "2", intermediate "1", and low-state "0" (c) The voltage transfer curves (VTC) and the respective short-circuit currents of  $T$ -CMOS inverter in comparison with CMOS at  $V_{DD} = 1$  V. The short-circuit currents are on linear scale for CMOS inverter and on log scale for  $T$ -CMOS inverter in off-state regime.

(GB) with multi-thresholds also can provide a route to the area-efficient back-end-of-line (BEOL) MVL integration for ternary full-adder circuit [16].

Since the mid of 2010s, device-level approaches have been intensively taken to achieve the compact STI design with number of components less than three (the number of logical states; *trit*). These MVL device technologies are summarized in Table I with each material/device type and operation mechanism [17]-[26]. Basically, multiple low and high threshold voltage ( $V_T$ ) are implemented in one single device for ternary operation. Then, this multiple switching device connected with one more component of complementary active or passive load in the series connection between  $V_{DD}$  and ground (GND) leads to the number of components (2) less than 3 (ternary states  $\{0, 1, 2\}$ ), which can accelerate the reduction of system complexity and number of interconnects as the information processing density increases.

Characteristics of MVL devices can be classified into step  $I$ - $V$  with constant current and multiple on-off switching with negative-differential resistance (NDR)/transconductance (NDT). To realize stable intermediate states for circuit-design available noise margin, multiple-step  $I$ - $V$  scheme with constant intermediate current is one of the promising device characteristics. For example, quantum-dot gate (QDG) FETs provided step-like transfer  $I$ - $V$  characteristics using Coulomb-blockade effect in QDG insulator as a pioneering work of ternary device research by Intel [17]. Recently, a new channel material of ZnO composite nanolayer has been demonstrated for MVL transistors with well-defined intermediate state by mobility edge quantization effect [18]. The number of steps in transfer  $I$ - $V$  curves can be controlled by stacking multiple ZnO layers.

The MVL devices based on the multiple on-off switching-oriented NDR/NDT characteristics have also been actively studied to resolve the inherent unstable intermediate state issue. Various NDR [19] and NDT

devices pursuing high peak-to-valley current ratio (PVCR) demonstrated ternary logic functions based on complementary graphene FET [20], 2D van-der-Waals heterojunction FET [21], ultra-thin body (UTB) MOSFETs [22], and organic heterojunction-based anti-ambipolar transistors [23], [24]. Recently, a quaternary ( $R = 4$ ) inverter function is demonstrated using double NDT characteristics by parallel configuration of WS<sub>2</sub>-graphene-WSe<sub>2</sub> heterojunctions with a p-channel transistor active load [25], which shows the possibility of compact thin-film stacking technology for the extension of multi-valued logic states as in [18].

### 3. STATUS AND FUTURE OF MVL DEVICE TECHNOLOGY

In contrast to all the previous MVL devices based on multi- $V_T$  scheme [17]-[25],  $T$ -CMOS with single  $V_T$  is an ultimately energy-efficient MVL device based on off-state working principle [26]. Specifically, ternary state operates in subthreshold region at  $V_{DD} < V_T$  and then, the complementary single-step  $I$ - $V$  can be implemented with  $V_{IN}$ -independent constant band-to-band tunneling current ( $I_{BTBT}$ ) and  $V_{IN}$ -dependent subthreshold current ( $I_{sub}$ ). Therefore, it can be demonstrated by the same layout design with conventional binary CMOS using the commercial foundry-processed 8-inch-wafers [26].

Figure 2(a) shows the measured transfer  $I_{DS}$ - $V_{IN}$  characteristics of  $T$ -CMOS where constant  $I_{BTBT}$  is clearly shown and exponentially varied by  $|V_{DS}|$  in off-current regime prior to the  $|V_{DS}|$ -independent  $I_{sub}$ . As in case of CMOS configuration,  $V_{DS}$  of  $T$ -nMOS ( $T_n$ ) is  $V_{OUT}$ , and  $V_{DS}$  of  $T$ -pMOS ( $T_p$ ) is  $V_{OUT} - V_{DD}$ . Thus, when  $V_{OUT}$  increases,  $I_{BTBT}$  of  $T_n$  ( $T_p$ ) increases (decreases) in complementary way and then, by Kirchhoff's law,  $V_{OUT}$  is determined at the same  $I_{DS}$  of  $T_n$  and  $T_p$ . For example, in lower  $V_{IN}$  ( $\sim 0$  V),  $I_{BTBT}$  of  $T_n$  and  $I_{sub}$  of  $T_p$  (black lines

in Figure 2(a)) generate high “2” state around 100 pA level short-circuit current. For  $V_{IN} = V_{DD}/2$ ,  $I_{BTBT}$  of  $T_n$  and  $T_p$  generate the intermediate “1” state (red lines) near 1 pA. In larger  $V_{IN}$  ( $\sim 1V$ ),  $I_{sub}$  of  $T_n$  and  $I_{BTBT}$  of  $T_p$  generate low “0” state (blue lines).

Figure 2(b) shows the measured output  $I_{DS}$ - $V_{OUT}$  curves, which clearly indicate that the complementary current component varies from  $I_{BTBT}$  ( $I_{sub}$ ) to  $I_{sub}$  ( $I_{BTBT}$ ) of  $T_n$  ( $T_p$ ) when  $V_{IN}$  increases from 0 to 1 V. It should be noted that the tunneling current,  $I_{BTBT}$  with exponential dependence on  $V_{OUT}$  determines each *trit* state {0, 1, 2}. Finally, as shown in Figure 2(c), the VTC and short circuit current of  $T$ -CMOS inverter are measured, which are distinguished from binary CMOS one having the same layout design. Conventional CMOS inverter achieves maximum current when both pull-up and pull-down are in on-state mode while the  $T$ -CMOS short-circuit current ranges in tunneling-based off-leakage regime. The exponential dependence of  $I_{BTBT}$  significantly reduces the static power consumption  $P_S$  ( $\sim I_{OFF}V_{DD}$ ) comparing with binary CMOS and previous MVL devices. Therefore, it allows the dynamic power ( $P_D$ )-dominant  $T$ -CMOS operation, which opens new circuit design field based on  $T$ -CMOS basic building block. Furthermore, single- $V_T$  scheme has advantages to scale down  $V_{DD}$  than previous multi- $V_T$  schemes and  $P_D$  ( $\sim V_{DD}^2$ ) could be further reduced by the half logic swing of  $V_{DD}/2$  in ternary operation.

The constant  $I_{BTBT}$  based on quantum-mechanical tunneling, which is the key mechanism of  $T$ -CMOS, has been observed in highly doped tunnel junction between the body and drain by halo and retrograde-well doping. Retrograde (low-to-high from surface to body) doping profile can be formed between source and drain with relatively high channel ion-implantation energy and dose. Then, the subthreshold diffusion current ( $I_{sub}$ ) becomes the exponential current component. As the first study, we proposed compact design of the STI operation based on the binary CMOS inverter having these two off-currents [27], [28]. By comparing with both numerical TCAD device simulation and analytical model equations, the feasibility of the  $T$ -CMOS operation has been verified in terms of the noise margin, off-leakage variation, and  $V_{DD}$  scaling.

In addition, we proposed  $T$ -CMOS device and circuit design platform based on compact model and verified the physical model parameters from the measured data [29]. The model parameters determine the VTC of STI with four noise margin voltages  $V_{IL}$ ,  $V_{IML}$ ,  $V_{IMH}$  and  $V_{IH}$ . The static noise margin (SNM) of STI is enhanced with  $T$ -CMOS design framework and power-delay product (PDP) analysis for high performance and low power ternary logic gates (STI, NMIN, NMAX) is provided.

Based on these prior works, we realized  $T$ -CMOS on large-scale 8-inch wafers using commercial CMOS foundries [26] which can significantly reduce power consumption as 1/1000 compared to binary CMOS.

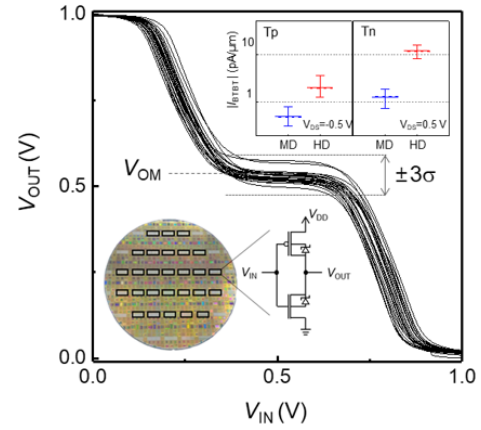


Figure 3. VTCs with die-to-die variations caused by  $\Delta I_{BTBT}$  and  $\Delta V_T$  from the 27  $T$ -CMOS inverters at  $V_{DD} = 1.0V$ . Inset shows photograph of 130-nm foundry processed 8-inch wafer with  $T$ -CMOS inverter schematic in 27 dies and the die-to-die variations of  $I_{BTBT}$  for 27  $T_n$  (MD) and  $T_p$  (HD) samples. MD/HD, medium/high dose.

From the foundry wafer-scale results, we verified that  $P_S$  and  $P_D$  are scaled down by reducing  $I_{OFF}$  to sub-picoampere level and scaling  $V_{DD}$  down to 0.5 V in the subthreshold regime. Furthermore, the intermediate state voltage of  $T$ -CMOS is more variation tolerant than binary CMOS subthreshold logic since it is reduced by log-scale of the constant tunneling current variations. We firstly demonstrated a *trit* state on an integrated circuit of the quantizer in ternary analogue-to-digital converter ( $T$ -ADC) and latch-cell operation in ternary static-random-access-memory ( $T$ -SRAM) on a silicon wafer to build ternary logic and memory systems. Thus, it could lead to ultra-low power ternary-binary hybrid circuit and system designs in semiconductors, which possibly inspire the software and algorithm engineers.

Now we discuss about the mass production results of  $T$ -CMOS technology by analyzing the variations of  $I_{BTBT}$ ,  $V_T$ , and VTC on wafer-scale measured data through the 130-nm and 90-nm CMOS processes. Figure 3 shows the measured VTCs of the  $T$ -CMOS inverters from 27 dies on an 8-inch wafer (inset). The third voltage state, output mid-state voltage ( $V_{OM}$ ), is formed at a half of  $V_{DD}$  by using voltage dividing between  $T_n$  and  $T_p$  with constant  $I_{BTBT}$ . Thus, the variation of the output mid-state voltage ( $\Delta V_{OM}$ ) is determined by the variation of  $I_{BTBT}$  ( $\Delta I_{BTBT}$ ). At this point, we should recall the unique exponential output characteristics of  $T$ -CMOS (Figure 2(b)), which lead to the logarithmic dependence of  $V_{OM}$  on  $I_{BTBT}$  by the simplified expression of  $V_{OM} \sim [1/\ln(1/I_{BTBT})]^2$ . From this relationship, the robust ternary inverter operation was experimentally demonstrated by the small standard deviation of  $V_{OM}$  ( $\sigma V_{OM} = 16$  mV) at average  $V_{OM} = 0.52V$ .

Despite its inherent robustness and tolerance to the variations, it is indispensable for suppressing  $\Delta I_{BTBT}$  as much as possible (i.e. within one-decade) to realize  $T$ -CMOS technology-based integrated circuits. From

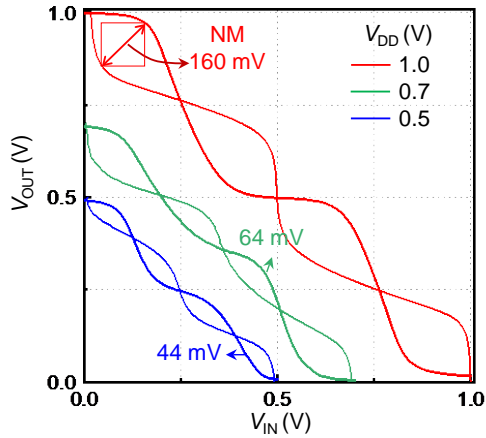


Figure 4. Butterfly curves from the symmetric  $V_{IN}$ - $V_{OUT}$  transfer characteristics at  $V_{DD}$  = 1.0, 0.7 and 0.5 V. The noise margin is the diagonal distance of the maximum possible square in symmetric VTC as noted in case of  $V_{DD}$  = 1.0 V.

the measured dataset of the  $T$ -CMOS devices on an 8-inch wafers, the observed values of  $\Delta I_{BTBT}$  were within one order of magnitude from MD to HD conditions (insets of Figure 3). This small  $\Delta I_{BTBT}$  can be explained by the relation to the junction effective doping concentration ( $N_{eff}$ ),  $\Delta I_{BTBT} \propto \exp(N_{eff}^{1/2}/N_{eff})$ . Thus,  $\Delta I_{BTBT}$  of  $T$ -CMOS will have much lower value with more increased  $N_{eff}$  by decreasing  $N_{eff}^{1/2}/N_{eff}$  term [30]. Further reduction of the  $\Delta I_{BTBT}$  can be obtained by exploiting an epitaxial doping which makes a more

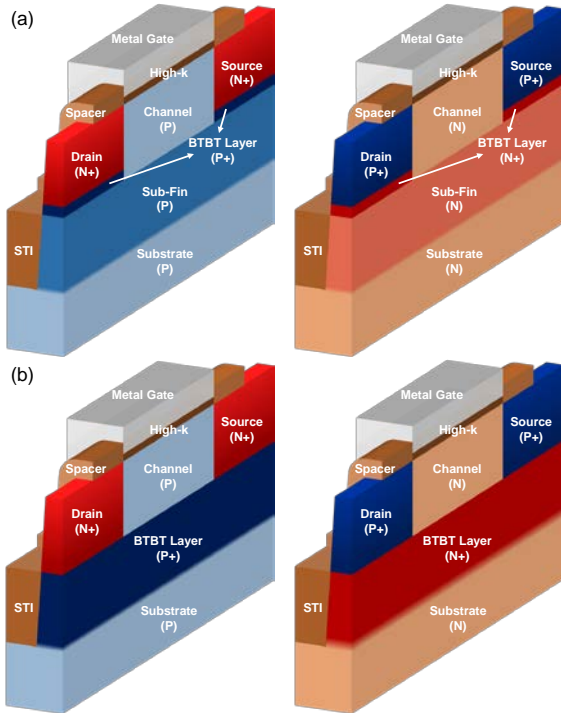


Figure 5. 3D cross-section view of  $T$ -n/pFinFET at the middle of fin with BTBT layer (a) just below source and drain locally and (b) at sub-fin region across the substrate. These examples can also be applied to 3D stacked nanowire and nanosheet structures for future sub-3nm technology node.

steeper doping gradient at tunnel junction. We also experimentally demonstrated the small variation of  $V_T$  ( $\Delta V_T$ ) by lowering the surface doping concentration [26]. The retrograde profile by a well-controlled epitaxial doping technique could also be a promising option for further suppression of the  $\Delta V_T$  and  $\Delta I_{BTBT}$ .

Figure 4 presents butterfly curves from the symmetric in-out VTCs with SNM evaluation for each  $V_{DD}$  = 1.0, 0.7 and 0.5 V. Compared with the butterfly curves in previous work [26], SNMs for  $V_{DD}$  = 0.7 and 0.5V have been improved by reducing GND noise with high-resolution source measure units (SMU). For the largest noise margin in the  $T$ -CMOS inverter, the ratio of input gate voltage ( $V_{IN}$ ) region for each  $T_n$  and  $T_p$  should have the optimal ratio of 3:1 for  $I_{BTBT}$  and  $I_{sub}$ , respectively. From this optimal  $T$ -CMOS design, the symmetric in-out VTC characteristics are obtained with a considerable SNM which is 25-45% of the ideal one ( $\sqrt{2}V_{DD}/4$ ) at  $V_{DD}$  = 1.0, 0.7 and 0.5V. Furthermore, the  $V_{DD}$  scalability for energy-efficient  $T$ -CMOS technology is proved by demonstrating symmetrically measured VTCs even at a scaled  $V_{DD}$  = 0.5 V.

Further enhancement of SNM can be achieved by reducing the subthreshold swing (SSW). Improving the gate controllability with tri-gate or gate-all-around (GAA) structure and negative capacitance (NC) effect of ferroelectric materials as gate dielectrics are promising schemes to enhance SNMs of  $T$ -CMOS inverters operating at a further scaled  $V_{DD}$ . Through a combination of the enhanced SSW and advanced doping technique, the ultimately scaled  $V_{DD}$  = 0.3 V operation can be expected in  $T$ -CMOS inverters with a considerable SNM.

For sub-10 nm  $T$ -CMOS technology, we propose advanced  $T$ -CMOS technology based on 3D FinFET structure in Figure 5, which show the 3D cross-section view of  $T$ -n/pFinFET at the middle of fin. In 3D structures such as FinFETs, highly doped BTBT layer can be formed locally just below source and drain by ion-implantation or epitaxial growth right before the regrowth of source and drain (Figure 5(a)) as well as by ground-plane (GP) ion-implantation, dopant-diffusion from Borophosphosilicate glass (BPSG), or a well-controlled epitaxial doping technique for sub-fin region across the substrate (Figure 5(b)), which offer a considerable design room for the tunnel junction area. Thus, in more advanced technology node,  $T$ -CMOS technology based on 3D FinFET and/or stacked nanowire (SNW) and nanosheet (NS) structure can also be implemented in the wafer-level integration using the already commercialized fabrication process techniques. Additionally, more robust power-scalable  $T$ -CMOS architecture can be realized with the reduction of  $\Delta V_T$  by lowering the influence of BTBT layer to surface channel region owing to the enhanced degree of freedom in the design of BTBT junction area.

The goal of the MVL technologies is to break through the power density limits while processing

larger amounts of data than binary system. Thus, the MVL device research will be conducted in the direction of power-scalability and 3D integrated technologies along with the wafer-level integration. In *T*-CMOS technology, robust power-scalable ternary system can be realized through a combination of low thermal budget epitaxial doping technology with abrupt graded junction and steep-slope transistors such as tunnel FETs (TFETs) and NCFETs with 3D-stacked architecture, which lead to the reduced SSW, increased design margin of junction area for  $I_{BTBT}$  and enhanced independent controllability of  $V_T$  and  $I_{BTBT}$ .

The multiple ZnO nano-layer or multi-threshold GB device based on 2D-layer stacking structure is an example of 3D-stacked device architecture that can be applied in low-thermal budget BEOL process. For NDT devices, lots of heterojunction devices composed of stacked 2D materials or organic semiconductor layers are developed and these kinds of thin-film process technologies will accelerate the power scalability of the MVL technologies for peta-scale information density era.

#### 4. CONCLUSION

Multi-valued logic (MVL) exploiting more than three logical bases, is a one of promising technology to breakthrough the binary Boltzmann switching CMOS facing power density limits by a reduced system complexity. Among various MVL technologies, the ultimately energy-efficient “sleeping-mode” working *T*-CMOS technology, which shows a commercial wafer-level integration feasibility with robust variation tolerance and power scalability, has been intensively investigated. For processing peta-scale information density by overcoming power scaling limits, the future direction of MVL technologies should be capable of providing 3D-stacked integration for area-efficiency as well as energy-efficiency by having supply voltage scalability. Based on the power-scalable and mass-producible MVL device platform technology, the collaboration with circuit and system level exploiting massively parallel processing architecture would open new research field for peta-scale ternary-binary hybrid system integration on semiconductors.

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