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Recent Developments in High Resolution Delta-Sigma Converters

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ABSTRACT

This review paper describes the overall operating principle of a discrete-time delta-sigma modulator (DTDSM) and a continuous-time delta-sigma modulator (CTDSM) using a switched-capacitor (SC). In addition, research that has solved the problems related to each delta-sigma modulator (DSM) is introduced, and the latest developments are explained. This paper describes the chopper-stabilization technique that mitigates flicker noise, which is crucial for the DSM. In the case of DTDSM, this paper addresses the problems that arise when using SC circuits and explains the importance of the operational transconductance amplifier performance of the first integrator of the DSM. In the case of CTDSM, research that has reduced power consumption, and addresses the problems of clock jitter and excess loop delay is described. The recent developments of the analog front end, which have become important due to the increasing use of wireless sensors, is also described. In addition, this paper presents the advantages and disadvantages of the three-opamp instrumentation amplifier (IA), current feedback IA (CFIA), resistive feedback IA, and capacitively coupled IA (CCIA) methods for implementing instrumentation amplifiers in AFEs.

KEY WORDS

Analog front end, capacitively-coupled instrumentation amplifier, continuous-time, delta-sigma modulator, chopper stabilization, discrete-time, switched-capacitor, analog-to-digital converter, excess loop delay.

1. INTRODUCTION

Currently, the use of wireless sensors offers new applications for medical devices and the Internet of Things [1], [2]. Wireless sensors should be designed with low-power consumption, small size, and low cost. Wireless sensors typically require low-power consumption because they are powered by batteries that cannot be easily replaced or recharged [2], [3]. The delta-sigma modulator (DSM) and analog front ends (AFE) are also undergoing changes due to this trend. This review describes the latest discrete-time delta-sigma modulator (DTDSM), continuous-time delta-sigma modulator (CTDSM), and AFE, which amplify small signals. Two types of DSMs can be implemented: continuous-time (CT) and discrete-time (DT) structures.

For the CTDSM, the coefficient depends on the capacitor and resistor. Therefore, the CTDSM is highly sensitive to process variations. To prevent the coefficient from changing due to the sensitivity of this process variation during actual testing, the trimming capacitor is considered when designing the actual chip. Among the factors that degrade the CTDSM's performance are clock jitter and excess loop delay (ELD).

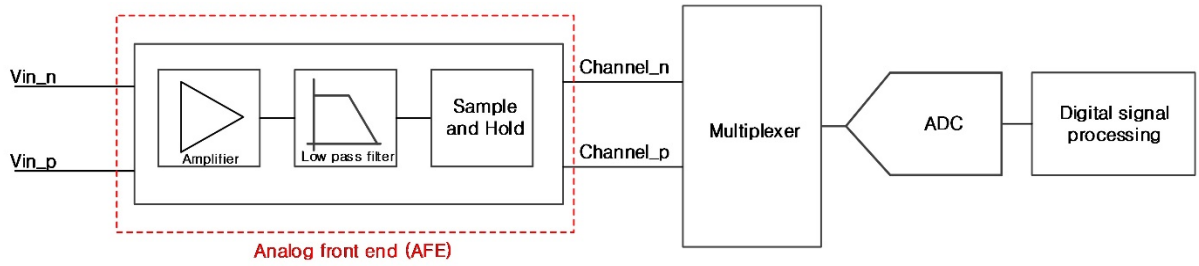

Figure 1. Conventional block diagram of the AFE

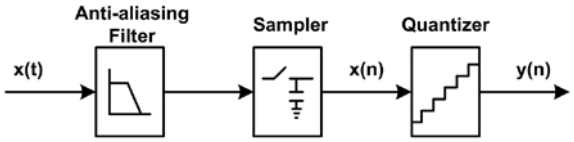

Figure 2. System block diagram of the analog-to-digital converter [4]

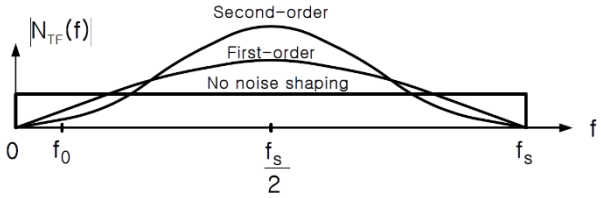

Figure 3. Comparison of the size of the noise transfer function according to the order [4]

The DTDSM, unlike the CTDSM, is generally implemented as a switched-capacitor (SC) circuit that is not sensitive to process variations. The DTDSM is also more robust against clock jitter and ELD problems.

The AFE has four topologies: the three-opamp instrumentation amplifier (IA), current feedback IA (CFIA), resistive feedback IA and capacitively coupled chopper IA (CCIA). Figure 1 shows an example of an AFE used to detect biomedical signals. Each channel has a set of preamplifiers, low-pass filters, and sample and hold circuits. The multiplexer selects one of the channel outputs and sends the channel output to the analog-to-digital converter (ADC).

Using a high-resolution DSM reduces the power loss of the AFE by removing the amplifier or reducing the power of the amplifier.

In this review paper, the ADC is briefly summarized and the latest trends in the development of DSM and AFE are explained in detail. Section II of this review provides a brief description of the analog-to-digital converter. Section III describes the delta-sigma modulator, and the latest studies that resolve the problems that occur in the DTDSM and CTDSM. Section IV explains the types of AFEs and their advantages and disadvantages and discusses the recent development trends. Section V presents the conclusions.

2. Analog-to-Digital Converter

In general, converters are divided into Nyquist data converters and oversampling data converters [4]. Nyquist data converters are vulnerable to variations in analog devices and various noises; therefore, there is a limit to realizing high resolutions. Therefore, oversampling delta-sigma data converter technology that can achieve a high resolution while overcoming these limitations is preferred.

The delta-sigma technique is a structure that modifies quantization noise. Assuming that the quantization noise is white noise, this technique is based on the principle of improving the signal-to-noise ratio (SNR) by reducing noise in the signal band [5].

As shown in Figure 2, it is a device that converts analog signals into digital signals through signal processing steps called sampling and quantization. The block at the front of the ADC is an anti-aliasing filter. During the sampling process, when the sampling rate is the same as the Nyquist rate, there is no signal distortion theoretically [5]. However, to solve the aliasing problem, an anti-aliasing filter that limits the maximum frequency component of the input signal before the sampling process is needed.

As the number of integrators of the modulator increases, the order of the noise transfer function (NTF) also increases. The $N_{TF}(z)$ of the L-order DSM can be expressed as follows:

$$N_{TF}(z) = (1 - z^{-1})^L \qquad (1)$$

Figure 3 shows the comparison of the size of the $N_{TF}(z)$ according to the modulator's order. As the order increases, the quantization noise component decreases in the low-frequency band, and noise shaping increases in the high-frequency band. The increased noise components outside the signal band f_0 are removed by passing through a low-pass filter (LPF).

3. Delta-Sigma Modulator Topology

High resolution ADCs for audio applications have traditionally been realized with multi-bit DSMs using SC circuits [6]. CTDSMs are also increasingly popular in

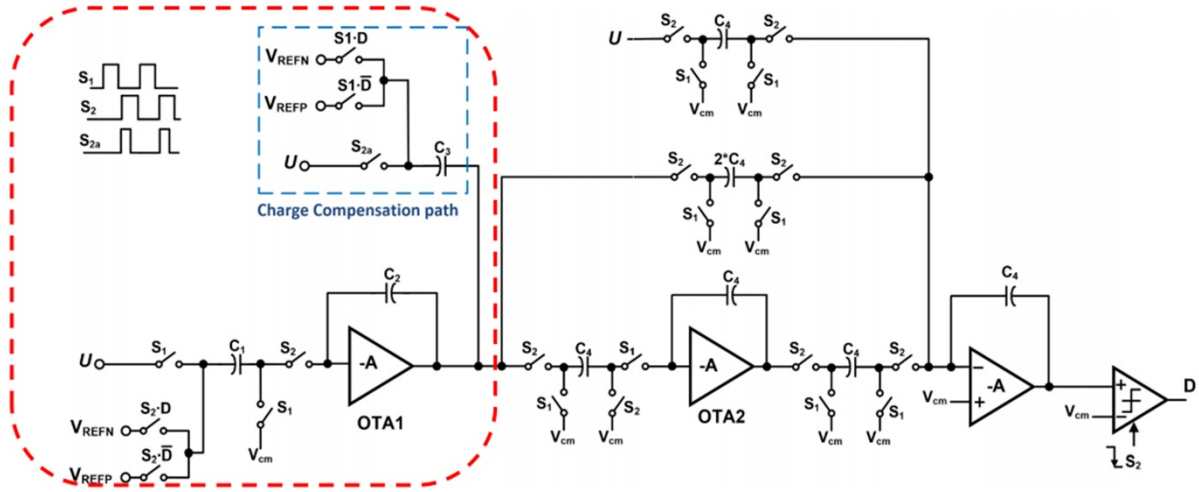

Figure 4. Second-order delta-sigma ADC with a compensation path in the integrator [13].

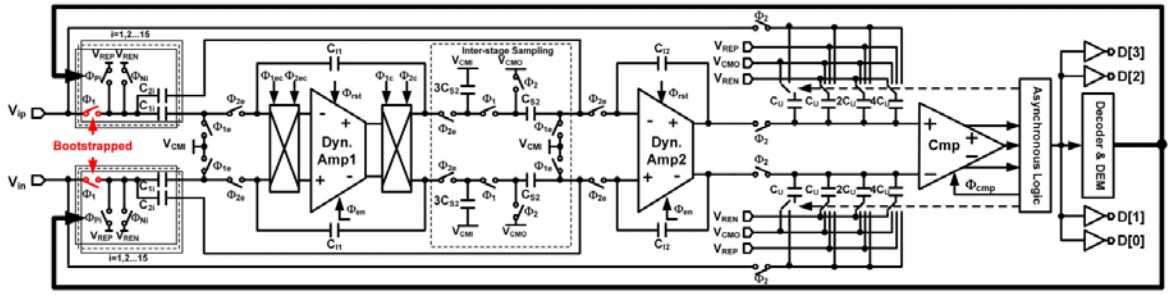

Figure 5. Discrete-time delta-sigma modulator using a dynamic amplifier [17].

these low-bandwidth applications due to their low-power consumption and ease of operation [7].

The CTDSM has several features, such as an intrinsic anti-aliasing filter, low-speed requirement of opamps, and low-power consumption [8]. Since the first integrator determines the noise and linearity performance of the CTDSM, it is inevitable that the first integrator consumes a large amount of power to meet the target noise and linearity. Therefore, designing a low-power CTDSM without compromising for noise and linearity is a difficult task.

A. Switched-Capacitor Delta-Sigma Modulator

The switched-capacitor circuit is a system that samples data and is a structure used when implementing DTDSM.

Low-power consumption is a key design criterion for medical devices. It is another approach used to reduce power by using a passive-SC integrator rather than the operational transconductance amplifier (OTA), which consumes a lot of power [9], [10]. The paper by A. F. Yeknami [11] discusses the use and effectiveness of a passive filter in a modulator with a focus on ultra-low speed and low-power applications. The implementation and measurement results of two low-power modulators using passive filters are described, and optimizations for power and performance are discussed.

The paper by Y. Yoon [12] presents a high-resolution dual-integrator DSM (DI-DSM) for low-power AFE circuits in biomedical devices. The AFE includes a preamplifier and a switched-capacitor delta-sigma ADC. The proposed DI-DSM adopts two types of clock frequencies. The first is the same as the existing frequency, and the other is half the existing frequency, providing a sufficient settling time for critical blocks. The proposed structure reduces harmonic distortion at the output of the preamplifier because the preamplifier is given enough time to charge the sampling capacitor in the DSM. Using a lower switching frequency in critical blocks significantly reduces the power consumption of both the preamplifier and the modulator.

The paper reviewed next shows a method of stabilizing nonlinearity caused by the slewing problem of the SC circuit while reducing power consumption. An adaptive bias technique is widely used to improve the stabilization accuracy of SC circuits [14]-[16].

The paper by M. Kareppagoudr [13] on slewing in the switched-capacitor circuit explains how to shorten the time available for linear settling, thus increasing nonlinear settling errors. This transient current demand can be met by increasing the bias current in the OTA; however, this significantly increases the static power consumption.

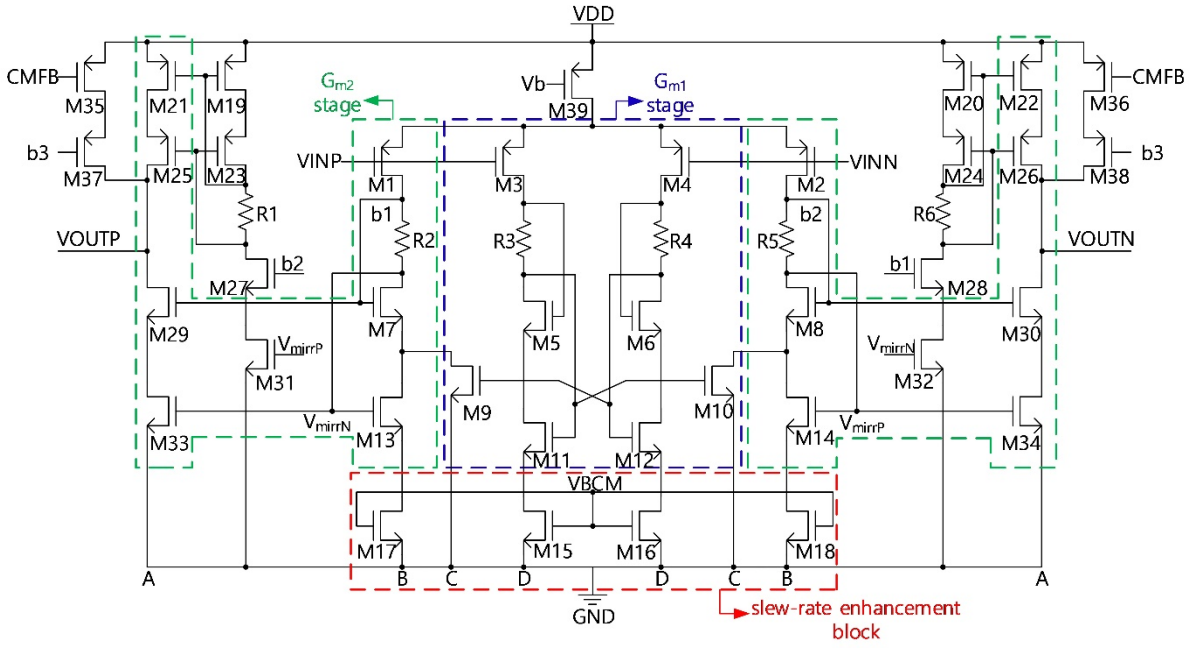

Figure 7. Slew-rate enhancement class-AB OTA [18].

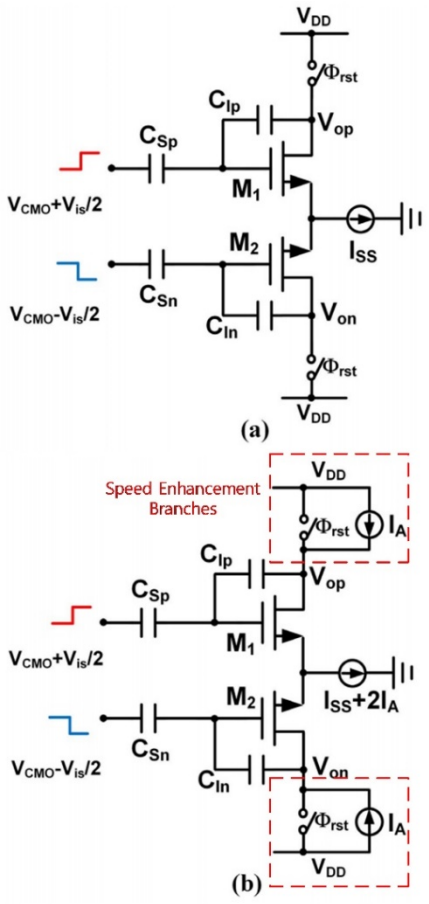

Figure 6. Dynamic amplifier during the transferring phase. (a) Without speeding up. (b) With the speed enhancement branches [17].

A slewing mitigation technique [13] is proposed in which an appropriate amount of charge is provided at the moment of switching the SC circuit so that the OTA does not need to provide a high peak current. This shows that slewing can be eliminated, and the OTA can be used with less static current for stabilization accuracy. Figure 4 shows the switched-capacitor single-bit second-order DSM with the charge compensation path applied.

The paper by S. Ma [17], which focuses on the modulator, proposes a new dynamic amplifier to realize switched-capacitor integration. The amplifier reset method is used to eliminate the common-mode voltage drop in the closed-loop dynamic amplifier during the integration phase without using additional load capacitance. Two auxiliary integrators are introduced to improve the integrator's settling rate. The inter-stage passive sampling network is shown as a dotted line in Figure 5. Figure 6(a) shows the proposed SC integrator in the transmission stage with a step voltage input. Figure 6(b) shows the common mode (CM) and differential mode (DM) coupling effect.

J. Kim [18], applied a slew-rate enhancement class-AB OTA to the first integrator of the SCDSM to improve performance. The proposed OTA in this paper adjusts the slew-rate enhancement transistor using an additional common-mode feedback loop, thereby solving the vulnerability of process, voltage, and temperature (PVT) fluctuations. Figure 7 shows the slew-rate enhancement class-AB OTA of the first integrator of the SCDSM. If the OTA slew-rate of the first integrator and the unity-gain bandwidth (UGBW) are low, harmonics are observed in the digital output spectrum of the SCDSM. For this reason, there is a good performance improvement by applying the slew-rate enhancement class-AB OTA to the first SCDSM integrator.

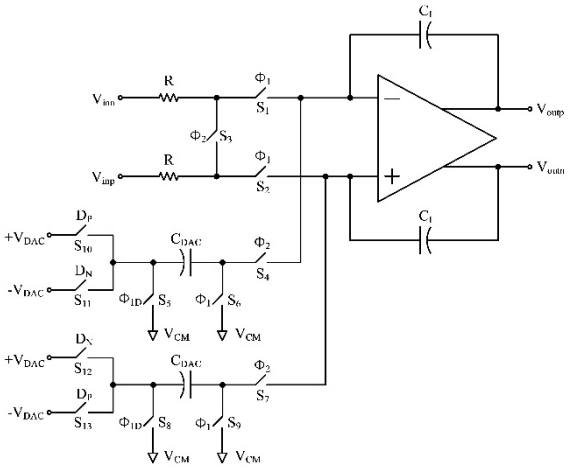

Figure 8. Proposed hybrid switching integrator [24].

To minimize power consumption, passive integrators are often used. However, passive operation reduces the SNR and causes NTF losses that attenuate the signal along the architecture, making thermal noise dominant [11]. Several active-passive hybrid implementations have been proposed to overcome the reduced loop gain problem in passive DSMs.

A. Hussain [19] describes how to use a low-gain amplifier and a passive switched-capacitor network to activate the SC integrator function. Compared to conventional opamp-based SC integrators, this solution uses a low-gain open-loop amplifier to drive a passive SC integrator with positive feedback. The open-loop amplifier requires a low DC gain and has exceptionally low-power consumption because it implements an embedded current adder. Power reduction for a single-bit can be achieved using a passive feedforward with a built-in adder to support the first amplifier. The small swing obtained at the output of the active block relieves the slew-rate requirement and improves linearity.

Next, the DSM based on the SC circuit has issues related to low-supply voltage. The nonlinearity of the input switch becomes more severe at low-supply voltages. The previous method used in the design of the low-voltage DSM included clock boosting technology [20], [21], bootstrapped switches [21], a switch RC integrator [22] and a mixed DDA integrator [23]. This technique is effective in increasing the linear range of the switch, but the disadvantage is the additional hardware required to generate higher voltage levels.

Y. Yoon [24] demonstrates the use of a hybrid switching integrator to operate at a 0.4V supply voltage without clock boosting or bootstrapped switches. The circuit proposed in Figure 8 has S_1 and S_2 switches through the input path. Because these switches are connected to the virtual ground of the OTA, they do not experience cumbersome changes in the switch-on resistance. In addition, all switches transmit a charge at a fixed DC voltage or virtual ground voltage using the SC DAC configuration during the ϕ_2 phase; thus, no distortion occurs. The proposed hybrid switching integrator is a DT integrator using resistance. Therefore, the output is similar to the timing of the operation of a mixed DDA integrator. A mixed DDA integrator is susceptible to switching noise because the input signal integration begins at the end of the ϕ_2 phase, while the proposed integrator begins integrating the input signal from the start of the ϕ_1 phase. Thus it helps overcome the switching noise effect that occurs when the ϕ_2 phase is completed.

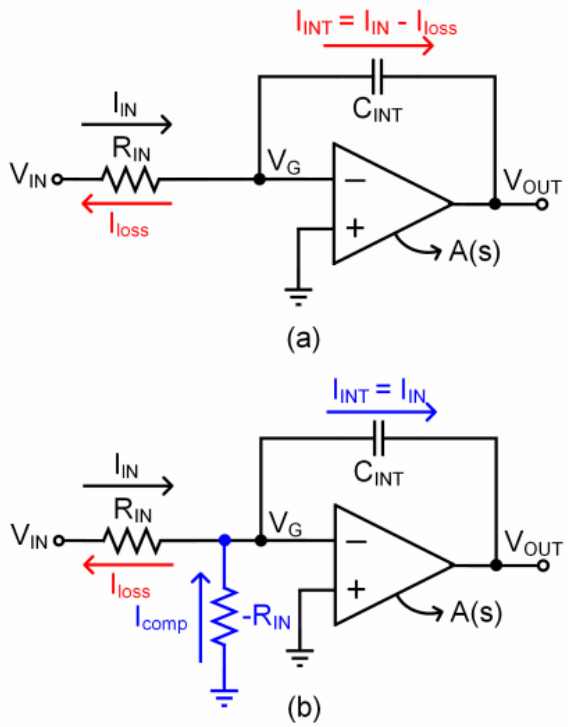

Figure 9. Operation of (a) an active-RC integrator and (b) a Negative-R assisted integrator [6], [35].

Finally, R. Wei [25] introduced a low-power delta-sigma capacitance-to-digital converter (CDC) for capacitive sensors [25]. The input capacitance range is extended by using zoom-in technology with an offset capacitor at the input of the capacitive sensor. Autozeroing technology is used in the OTA to reduce offset and noise.

B. Continuous-Time Delta-Sigma Modulator

The initial implementation of the delta-sigma ADC used a CT circuit, but after the SC circuit was developed, it was primarily implemented using SC technology [5]. However, the recent trend in high-speed applications has shifted the focus back to CT circuits [26]. One of the advantages of the CT circuit is that it does not require a switch; thus, CTDSM can be used for low-voltage designs. Since there is no switch, the stabilization requirements of the amplifier are relaxed, and power consumption can be reduced compared to the DT structure. A power-efficient low-voltage CTDSM is described in [27]. There are several ways

to reduce power consumption. Among them, J. L. A. de Melo [28] describes energy and area efficient technologies for the CTDSM. This technique is based on increasing the contribution of a single-bit comparator to the loop-gain by using a passive RC integrator with a low-gain amplifier in a CTDSM loop filter.

Several implementations have been investigated in recent years to improve the energy efficiency of the CTDSM [29]-[34]. A multi-bit quantizer is used mainly to reduce the phase size of the feedback DAC signal [29], [33], [34], and to alleviate the linearity requirement of the first integrator. However, the mismatch of the unit elements of the feedback DAC requires dynamic element matching (DEM), which limits the linearity performance of the CTDSM, increases the design complexity, and leads to higher power consumption. In contrast, a single-bit quantizer whose feedback DAC is essentially linear, simplifies the design and reduces power consumption [7], [8], [30]-[32].

M. Jang [6] found that the opamp of the CTDSM integrator has stringent noise and linearity requirements, resulting in large-power losses. Thus, the solution is to reduce the power drastically by applying a negative-R assisted integrator to alleviate the opamp requirements, including DC gain, UGBW, thermal noise, 1/f noise, and linearity.

Figure 9(a) shows the operation of the active-RC integrator. The finite response of opamp A(s) makes the virtual ground non-ideal (V_G=0) and causes current loss I_{loss}. As a result, the integration current I_{INT} (=I_{IN}-I_{loss}) loses its size and bandwidth due to the finite gain and bandwidth of the opamp, resulting in the loss of the integrator. In contrast, Figure 9(b) shows the operation of the negative-R assisted integrator. When negative-R is applied to the virtual ground, the compensation current I_{comp} is generated at the ground, canceling I_{loss} and effectively making the virtual ground ideal (V_G=0). Therefore, the integrator's I_{loss} due to the opamp's finite gain and bandwidth is compensated for, and I_{INT} becomes the same as the input current I_{IN}.

An integrator typically has three structures: opamp-RC, OTA-RC, and G_m-C. The opamp-RC integrator has good linearity but has a significant drawback, which is the output swing. To make the output impedance small with a complementary metal-oxide semiconductor (CMOS), a source follower structure must be used. In this case, the output swing increases. The OTA-RC integrator has the advantage of not being affected by linearity or parasitic capacitance. The disadvantage is the finite DC gain. The G_m-C integrator structure has the advantage of being fast, easily adjustable, and low in current consumption. The disadvantage is that the coefficient can easily change owing to the influence of nonlinearity and parasitic capacitance. The advantages and disadvantages of each structure mentioned are provided in [5].

D. Basak [36] examines the delta-sigma using the G_m-C integrator structure. Traditionally, G_m-C-based DSMs are limited in performance due to the nonlinearity of G_m circuits. To obtain sufficient linearity, source degeneration is generally applied to G_m circuits, which inevitably reduces the transconductance and thermal noise efficiency of G_m circuits. Thus, this paper [36] presents a new way to change this paradigm. First, a DSM with a passive RC LPF is applied to the feedback. By placing the cut-off frequency of the LPF at the edge of the signal band, the pole of the DSM loop filter reduces the power consumption. The LPF also suppresses the high-frequency component of quantization noise so that quantization noise is not captured in the signal band while using a nonlinear G_m circuit in the feedback of the DSM. By matching the transmission characteristics and inputs, the input and feedback G_m circuits cancel nonlinearity with respect to each other. Second, an integrated input feedback G_m circuit with shared degeneration resistors is proposed, which has high transconductance and noise efficiency and at the same time allows for large input and feedback signals. L. Lv et al. [37] also used the G_m-C structure design.

C. Excess Loop Delay and Clock Jitter

Before conducting a detailed analysis of the effects of ELD, the effect of delay on the ELD should be considered. Both the DTDSM and CTDSM have ELDs. This timing error is a problem only in the CTDSM because it is continuously accumulated by the integrator through the DAC of the feedback loop. The ELD increases the noise floor and severely reduces the SNR of the DSM [38]. This leads to the instability of the DSM. Even exceedingly small amounts of ELD can cause instability in high-speed modulators [39]. Therefore, it is essential to ensure the stability of the closed-loop DSM. As with all feedback loops, adding a delay reduces the modulator stability. In addition, modulators with higher order or higher out-of-band gain are more sensitive to the effects of excess delay. Finally, because the size of the loop gain does not change according to the delay, the suppression of quantization noise in the signal band should not be affected. Fortunately, the serious consequences of delay can be easily solved by adjusting the coefficient of the loop filter and adding a direct path around the quantizer [5]. Given the excess delay t_d, the modified coefficient can be easily determined. This paper discusses ways to compensate for these ELD effects as much as possible [40]-[43].

T. He [42] proposes a small delay DSM truncator circuit. The truncator feedback path is merged with an ELD compensation loop that controls the reference selection of the internal quantizer. This method solves

the ELD problem by embedding a truncator in the digital ELD compensation path without adding to circuit complexity.

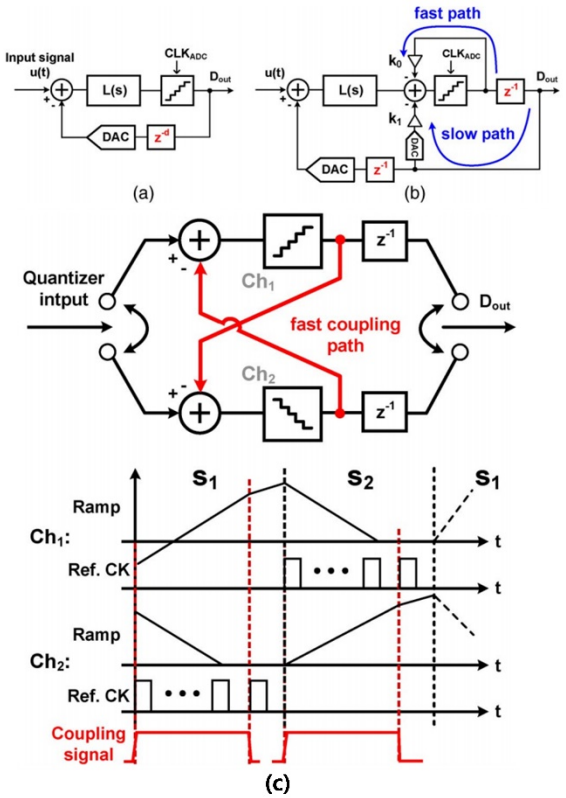

Figure 10. (a) CTDSM with a d-cycle of ELD. (b) Theoretical solution for two cycles of ELD compensation using a fast/slow path. (c) Proposed channel coupling for a fast compensation path [41].

S. Kim [43] implemented ELD compensation with a capacitor-based voltage (CV) DAC for ELD compensation that is less affected by PVT than modulators using other ELD compensation schemes.

J. Guo [40] presents a new compensation algorithm for the ELD of CTDSM ADC based on a model matching method to improve system performance with the same loop filter. Compared to the previous compensation method, the model matching algorithm is more practical because the ELD values change randomly with each clock cycle.

Another way to complement ELD is described in [41].

The paper by Y. Hu [41] describes CTDSM using a dual-slope time interleaved quantizer. The ELD of the two sample clocks is compensated using the time information provided through interleaved channel coupling. As a result, one full clock cycle is provided for the digital-to-analog conversion dynamic element matching (DEM) operation, allowing for digitally synthesized DEM blocks. Figure 10(a) shows the theoretical solution for two-cycle ELD compensation using the ELD's d-cycle, and Figure 10(b) shows the high-speed/low-speed path. In Figure 10(c), because one channel of the time-interleaved quantizer (TIQ) is in the discharging phase, time information representing the quantized signal value is sampled and transmitted to the other channel. Channel coupling using dual-slope time information can be performed simply by using a current-source turned on or off by dual-slope logic. No additional timing steps or explicit DAC work is required. Since the channel coupling operation directly affects the next sample of TIQ, a rapid ELD compensation loop is realized.

4. Analog Front End

The AFE amplifies a small signal and passes it to the DSM. When amplified, noise contained in small signals is also amplified; therefore, care must be taken to remove noise. To implement IA, there are traditionally four topologies: three-opamp IA [44]-[46], current feedback IA [47], resistive feedback IA [48], and capacitively -coupled chopper IA [49].

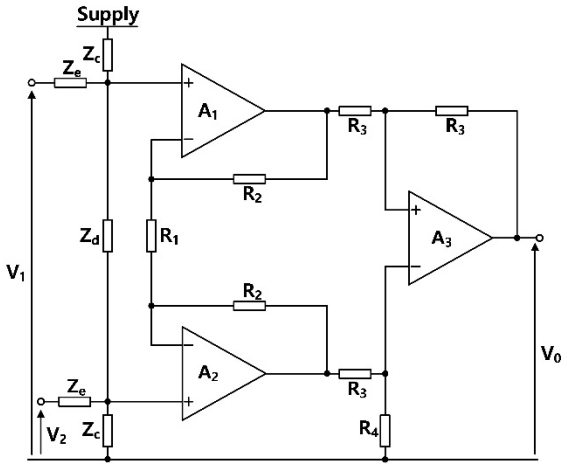

Figure 11. Instrumentation amplifier [45].

A. The Three-Opamp Instrumentation Amplifier

The three-opamp topology has high input impedance and excellent linearity, as demonstrated by [44]-[46]; however, the power efficiency is reduced because two low-noise input amplifiers are required. In addition, the three-opamp IA cannot detect the rail because the input common-mode voltage must also be within the range of the output voltage of the input amplifier. Figure 11 shows the instrumentation amplifier.

B. The Current-Feedback Instrumentation Amplifier

Current-feedback IA (CFIA) also has high input impedance as shown by [47]; however, gain accuracy is limited due to a mismatch between input and feedback transconductance. Figure 12 shows the current feedback instrumentation amplifier. The CFIA can have a rail detection function using an n-channel metal-oxide semiconductor (NMOS) or p-channel metal-oxide semiconductor (PMOS) based input differential; however, it is very difficult to achieve the rail-to-rail input

function with high gain accuracy because the mismatch between the input and feedback transconductance is generally also a function of the input CM voltage. The power efficiency of CFIA is also limited by the need for two input and feedback transconductances.

C. Lee [50] presented low-noise, low-power, chopper-stabilization, and a CFIA for biopotential signal acquisition applications. The design used includes an AC coupled chopper stabilization CFIA to reduce 1/f noise. It also uses a switched-capacitor integrator to reduce the input offset and provide high accuracy.

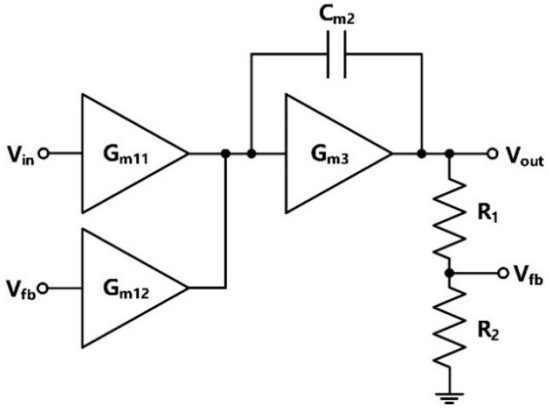

Figure 12. Schematic of the current-feedback instrumentation amplifier [47].

C. The Resistive-Feedback Instrumentation Amplifier

Resistive-feedback IA topology is the third option, however, as noted in [48], the value of the input resistance is a trade-off between noise and input impedance. Finally, the closed-loop gain of the three topologies is defined by the resistive network loading the output stage of the IA [51]-[54]. Increasing the resistance of the network leads to a larger chip area and more noise.

D. Capacitively-Coupled Chopper-Instrumentation Amplifier (CCIA)

The CCIA is used in [49], [55]. Compared with IA based on the three existing topologies mentioned, the CCIA has the advantage of a rail-to-rail sensing capability, high power efficiency, high gain accuracy, and suitability for a low-power design. However, there are two disadvantages: a limited input impedance determined by the equivalent resistance due to the main $C_{in1,2}$ and f_{chop}, an up-modulated offset of G_{m1}, 1/f noise, and a chopping ripple. Using a positive feedback loop (PFL), ripple reduction loop (RRL), and DC servo loop (DSL) resolve these disadvantages. Figure 13 shows the CCIA. It is based on a two-stage Miller compensated opamp composed of an integrator built around the input transconductance G_{m1} and G_{m2}. Figure 14 shows that the CCIA compensates for the two drawbacks mentioned with PFL, RRL and DSL.

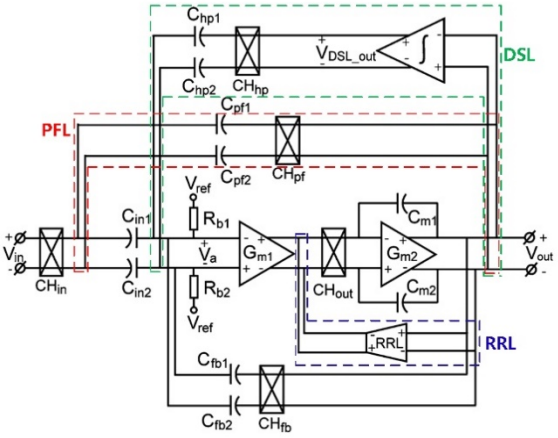

Figure 13. A schematic of the capacitively-coupled chopper instrumentation amplifier [49].

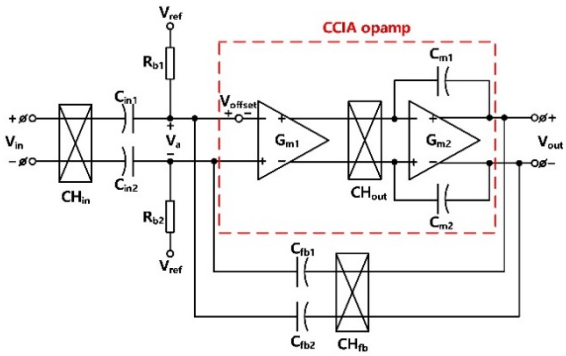

Figure 14. A block diagram of the capacitively-coupled instrumentation amplifier with the optional DC servo loop [49].

5. CONCLUSION

This review paper describes the basic working principle of ADCs. In addition, the basic operating principles of the DTDSM and CTDSM, and their advantages and disadvantages are explained. Each DSM is reviewed through recent papers based on advanced techniques. This paper describes how to solve the problem of slewing and the low-voltage switch that occurs when the DTDSM switched-capacitor circuit is used. To design a DTDSM with low power, a DSM uses a passive filter. A method to improve DSM performance using the slew-rate enhancement OTA of the first integrator of the SCDSM and a method for improving performance using a dynamic amplifier have been described. Another method uses negative-R to reduce the power consumption of the CTDSM. In addition, the power can be reduced using the G_m-C integrator structure. This paper also describes various methods used to resolve the CTDSM's clock jitter and ELD, including a method used to resolve the ELD problem with a new algorithm, and another method using a dual-slope time interleave. AFEs are also described, which are widely used in medical device sensors. They amplify small signals. As noise is also amplified during amplification, low-frequency noise is

removed using chopper-stabilization techniques. The AFE is described based on the advantages and disadvantages of the 3-opamp IA, CFIA (current feedback IA), resistive feedback IA and capacitively coupled IA (CCIA) methods.

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