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Brief Overview on Design Techniques and Architectures of SAR ADCs

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ABSTRACT
Successive Approximation Register (SAR) Analog-to-Digital Converters (ADC) seem to become the hottest ADC architecture during the past decade in implementing energy-efficient high performance ADCs. In this overview, we will review what kind of circuit techniques and architectural advances have contributed to place the SAR ADC architecture at its current position, beginning from a single SAR ADC and moving to various hybrid architectures. At the end of this overview, a recently reported compact and high-speed SAR-Flash ADC is introduced as one design example of SAR-based hybrid ADC architecture.

KEY WORDS
SAR ADC, asynchronous SAR ADC, loop-unrolled SAR ADC, decision redundancy, digital error correction, multi-bit/cycle SAR ADC, hybrid SAR ADC, pipelined-SAR, sub-ranging SAR, flash-SAR, noise-shaping SAR.

1. INTRODUCTION
Owing to the digital-friendly compact architecture and the advanced modern CMOS technologies providing high-speed transistors and good device matching characteristics with fine feature sizes, SAR ADCs have become a very popular ADC architecture during the last decade. Figure 1 shows this design trend with ADCs presented in the International Solid-State Circuits Conference (ISSCC) and the Symposium on VLSI Circuits (VLSI) during the recent twenty years [1]. Aside from the improved performances of the ADCs presented in 2010 – 2020 compared with the ones in 2000 – 2009 in terms of signal-to-noise-plus-distortion ratio (SNDR) as well as the highest input frequencies (f_{in_hf}) and the aperture accuracy (jitter), we clearly notice that SAR ADCs have become a dominant architecture during the period of 2010 – 2020. While the pipelined architecture was dominant in 2000 – 2009, majority designs showing f_{in_hf} ranging from several MHz to several hundreds of MHz and SNDR ranging from 40dB to 80dB, recently, such performance targets could be achieved with

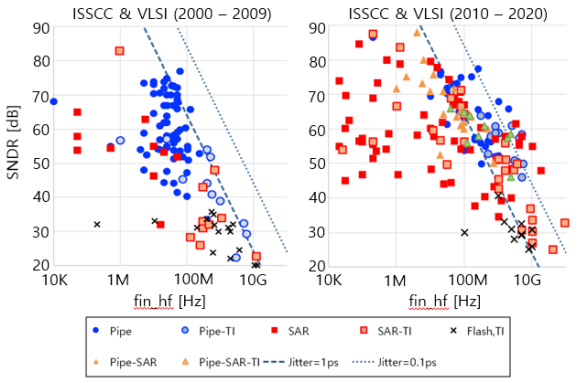

Figure 1. Trends of ADC architecture choice and performances based on [1].

SAR-based ADCs including pipelined-SAR ADCs. Moreover, recent SAR-based ADCs show very wide performance spectrum, f_{in_hf} ranging from tens of kHz up to tens of GHz and SNDR ranging from 30dB to around 85dB. The energy consumption (P/f_{snyq}) shown in Figure 2 also reveals the low-power advantage of

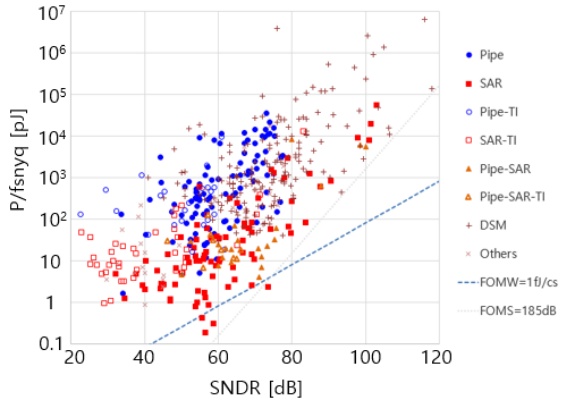

Figure 2. ADC performance trends (P/fsnyq – SNDR) [1].

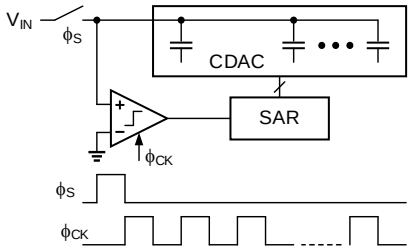

Figure 3. Basic structure of a synchronous SAR ADC.

SAR ADCs, especially when SNDR is lower than 80dB.

This boom of SAR ADC is attributed not only to evolution of the improved process technologies but also to the innovations in circuit techniques and architectures. In this paper, we will study how SAR ADCs have been evolved by reviewing various design techniques and architectures that have significantly contributed to advance of SAR ADC performance.

2. ADVANCED SINGLE SAR ADC

A. Asynchronous Decisions

Compared with traditional pipelined ADC architecture whose performance used to heavily rely on power-hungry operational amplifiers, SAR ADCs do not require such a burdensome analog building blocks. They need only a single comparator and a capacitor digital-to-analog converter (DAC) as analog building blocks as illustrated in Figure 3. This compact and digital-friendly structure makes SAR ADCs very suitable for scaled CMOS technology. Such a structural advantage could even make it possible to design SAR ADCs utilizing the well-established digital design methodologies [2]. One drawback of a typical synchronous SAR ADC is the slow conversion speed due to the 1b/cycle decision principle. This requires a much higher internal clock frequency for the comparator (ϕ_{CK}) than the clock for input sampling (ϕ_S). One more drawback of a synchronous SAR ADC would be that there could be considerable time wasting in each comparator decision phase: even if the comparator's latching is completed early by a large input signal [3], no other operation would be conducted until the next clock period begins. Such drawbacks related to the comparator clock could be solved efficiently by the asynchronous SAR ADC architecture shown in Figure 4, where the comparator clock is self-generated as soon as the latching is completed. In [4], it is estimated that the total time required for comparator decisions in an asynchronous SAR ADC can be reduced to be almost half compared with a typical synchronous SAR ADC when the ADC resolution is assumed to be sufficiently high. One drawback with asynchronous design is the comparator metastability. In order to alleviate this problem, metastability reduction techniques can be utilized as in [5].

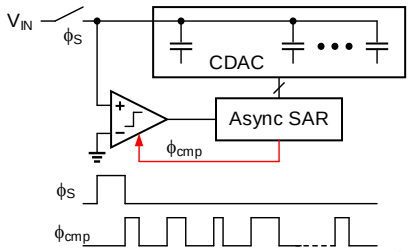

Figure 4. Asynchronous SAR ADC having a self-generated comparator clock.

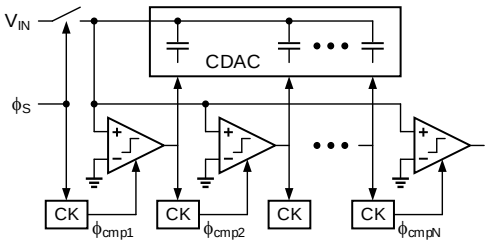

Figure 5. Basic structure of a synchronous SAR ADC.

In order to further reduce the conversion time, we can eliminate the reset time of the comparator by utilizing multiple comparators. Two alternating comparators in [6] could hide the reset time of one comparator behind the conversion period of the other comparator. More advanced architecture would be the loop-unrolled structure [7], where each comparator is dedicated to each capacitor DAC (CDAC) element switching, eliminating the need of DAC switching logic as illustrated in Figure 5. Many SAR-based high-speed ADCs could be implemented by utilizing this architecture, like [8]. One clear drawback with the loop-unrolled architecture is that each comparator requires offset calibration and it often becomes considerable size burden.

B. Low-power Design Techniques

Various circuit techniques could further enhance the low power advantage of SAR ADCs. Many researches have been conducted to save the CDAC switching power consumption [9]-[19]. Some even could

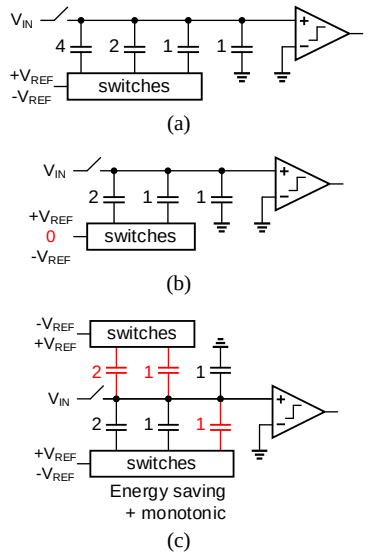

Figure 6. (a) conventional CDAC, (b) V_{CM}-based switching CDAC, and (c) Energy-saving + monotonic switching CDAC.

achieve the Walden Figure-of-Merit (FoM) [20] lower than 1 fJ/conversion-step [18], [19]. Unlike the traditional SAR ADC architecture with two voltage references, shown in Figure 6(a), the V_{CM}-based switching scheme proposed by [11] (also by [12] and [13] independently), shown in Figure 6(b), could reduce the total capacitance of the CDAC by half owing to the additional reference of V_{CM} (noted as "0" in the figure). Owing not only to the reduced capacitance but also to the reduced switching step size as well as the removed switching-back operation [13], the V_{CM}-based CDAC switching could achieve excellent energy efficiency and become popular for low power design. One drawback with the V_{CM}-based switching scheme might be the difficulty in designing low resistance switch for V_{CM}. The monotonic switching technique [14] can eliminate the need of V_{CM} by the asymmetric CDAC switching but the scheme has a varying common-level problem. The energy saving switching technique [10] could implement V_{CM}-based-like switching behavior without utilizing V_{CM} by splitting each capacitor by half as shown in Figure 6(c).

Improved process controllability of advanced CMOS technologies also contributed in reducing CDAC switching power consumption by reducing the minimum unit capacitor values without the need of dedicated process for capacitor implementation [21]. In [22], a CDAC with a metal-finger structured 0.25-fF unit capacitor could achieve 12b linearity. One drawback with the metal-finger unit capacitor would be the top-plate parasitic capacitance which is comparably as large as the bottom-plate parasitic. This attenuates the CDAC signal significantly and becomes burden to the comparator noise design. The pillar-shaped unit capacitor structure shown in Figure 7 could alleviate this top-plate parasitic capacitance problem efficiently by enclosing the top plate with the

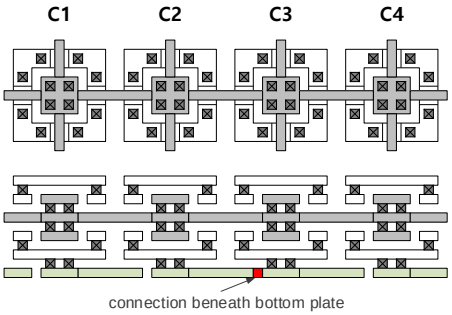

Figure 7. Array of pillar-shape capacitors: top view (upper), side view (lower).

bottom plate [23]. In addition, by connecting the interconnection metal beneath the bottom-plate, as the lower part of Figure 7 illustrates, [23] could implement well-matched capacitors regardless of interconnection and showed a 12-bit linearity with 0.58fF unit capacitors.

As more power should be burnt for less noise in a comparator and as a single fixed comparator should work for the entire decision cycles in a SAR ADC, power consumption by a comparator becomes more considerable as the ADC resolution gets increase. Comparator's power consumption can be reduced by allowing some errors during the decisions of MSBs and by correcting them in digital domain with the redundancies added in the LSBs decisions, as in [24]. Allowing decision errors with redundancies not only saves comparator power consumption but also enhances the SAR conversion speed by reducing the DAC settling time as will be discussed in the followings.

C. Error Tolerant Designs

Due to the irrevocable decision process of the basic successive approximation (SA) algorithm, CDAC settling at every decision cycle should be sufficiently accurate and this settling requirement makes SAR ADCs slow. Decision redundancies, however, can allow some amount of decision errors during MSBs decisions and digital error correction can correct the error. Therefore, the digital error correction can enhance the conversion speed with fast DAC settlings even though the entire number of decision cycles increases by that [13], [25]-[29]. While binary-weight based conversions would be more natural for SAR ADCs, dedicated cycle(s) for redundant decision(s) should be inserted between normal conversions [25]-[27]. A nonbinary-weighted SAR ADC can insert redundancies between (almost) every design cycles. The circuit implementation of the first nonbinary SAR ADC [28] was quite complicated because of the sub radix-2 implementation. However, the simple integer-based nonbinary CDAC design method proposed in [29], beginning from a binary CDAC and splitting some large capacitors into smaller binary weighted ones as illustrated in Figure 8, could make nonbinary

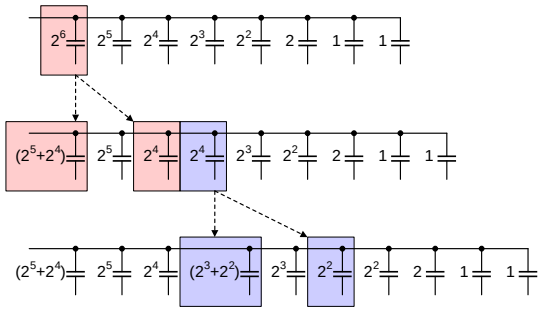

Figure 8. Simple binary-to-nonbinary CDAC conversion procedure.

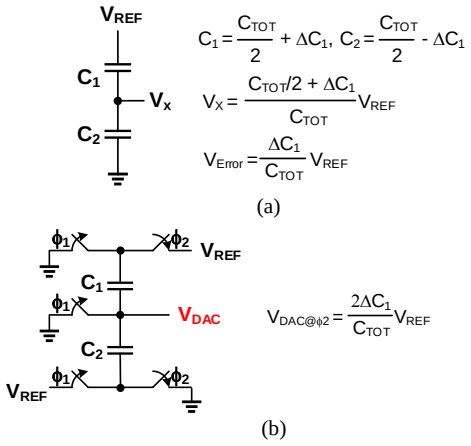

Figure 9. (a) Error voltage on CDAC by capacitor mismatch and (b) a circuit technique to readout the mismatch amount.

CDAC implementation as simple as it can be auto generated [2].

Judging from recent publications, ADCs with resolution higher than 12b seem to require linearity calibration. Even though numerous linearity calibration methods have been developed since the first self-calibrating SAR ADC introduced in [30] and [31], the key idea in [31] is still utilized in many recent CDAC linearity calibration schemes, as in [32]. Figure 9 explains how capacitor mismatch appears at the output of a CDAC and how we can measure the mismatch from an actual circuit according to [32]. While two capacitors of C_1 and C_2, which are supposed to be matched, have mismatches of ΔC_1, the CDAC output (V_X) will have an error voltage (V_{Error}) of $(\Delta C_1/C_{TOT})V_{REF}$ (Figure 9(a)). But as V_{Error} cannot be measured alone from V_X, a circuit configuration shown in Figure 9(b) was invented: During ϕ_1, C_1 is fully discharged while C_2 is charged with V_{REF}. When ϕ_2, the switching changes so that C_1 is charged with V_{REF} and C_2 is discharge and V_{DAC} stays at 0. However, if $C_1 \neq C_2$, V_{DAC} will deviate from 0 by $V_{DAC} = (2\Delta C_1/C_{TOT})V_{REF}$. As the error voltage on V_{DAC} by ΔC_1 will not be large, a relatively low-resolution ADC, actually the LSB part of the ADC itself, can be utilized to readout the error without a concern of capacitor mismatch. The actual capacitor mismatch amount of each capacitor can be extracted by dividing the output

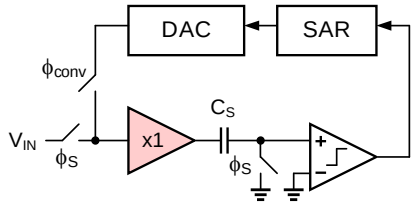

Figure 10. SAR ADC with loop-embedded input buffer.

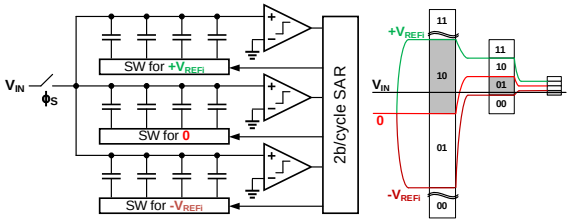

Figure 11. 2b/cycle SAR ADC architecture in [37].

code by 2. The capacitor error can be compensated whenever the capacitor is utilized by generating a compensating voltage utilizing the same DAC.

Nonlinearity is generated not only from the DAC but also from the input buffer. While the power consumption of a SAR ADC itself can be very small, an ADC input buffer needs to have a stronger driving capability compared with one for pipelined ADC because of the much shorter input sample time. This becomes a serious burden to the input buffer. The linearity requirement of the input buffer can be significantly relaxed by utilizing the loop-embedded input buffer structure shown in Figure 10. It has an input buffer in the loop of the SAR ADC so as for the DAC to suffer from the same nonlinearity and, thus, to effectively cancel out the nonlinearity of the input buffer. One caution with this structure is the parasitic capacitance of the switch placed between the DAC and the input buffer. As the parasitic junction capacitance of a switch degrades the CDAC nonlinearity, the original high-speed designs in [33] and [34] utilized a current-steering based voltage DAC. When the conversion speed is relatively low as in [35] and [36], however, a CDAC can still work with high linearity above 12b owing to the relaxed on-resistance requirement for the DAC settling.

3. HYBRID ARCHITECTURES

A. Multi-bit/Stage SAR ADCs

The limited conversion speed of a typical 1b/cycle SA decision can be improved by achieving multiple bits at each decision at a cost of increased hardware burden. Figure 11 illustrates one representative structure of a 2b/cycle decision SAR ADC [37]. Three parallel SAR ADCs are utilized to generate three decision thresholds at each cycle for a 2b flash ADC like operation. In order to reduce this hardware burden by the CDACs, several techniques have been proposed.

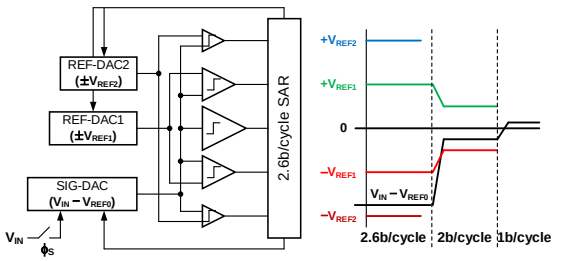

Figure 12. 2.6b/cycle SAR ADC structure in [44] and its tapered resolution operation.

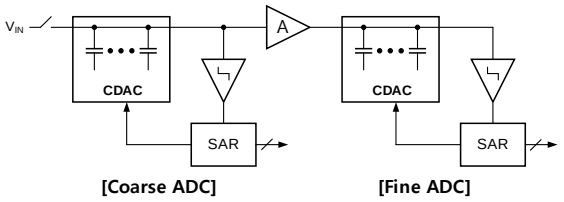

Figure 13. Simplified block diagram of a pipelined SAR ADC.

A shared resistor-string based DAC (RDAC) [38] and interpolation techniques [39], [40] could simplify the structure by reducing the number of CDACs. The interpolation technique could later extend the resolvable resolution per cycle up to 3 bits [41]. One drawback with the multiple CDACs is the limited sampling bandwidth due to the increased input capacitance. This problem could be eliminated by splitting CDACs into reference generation DACs (REF-DACs) and an input sampling and residue generation DAC (SIG-DAC), as in [42]. The nonbinary decision of [42] could achieve a robust performance of 6.6 effective number of bits (ENOB) from the 7b output design, and that structure was further improved for higher resolution with reduced resolution per cycle (tapered resolution) with redundancies to overcome the comparator offset problem as decisions go down to the LSBs [43], [44]. Figure 12 shows the structure of a 2.6b/cycle SAR ADC architecture, proposed in [44]. The tapered resolution from 2.6b/cycle to 2b/cycle and lastly to 1b/cycle could correct the comparator-offset-induced decision errors, and the four-channel time-interleaved design achieved a 10b 1.7GS/s performance with an outstanding FoM of 30.4 fJ/conversion-step.

B. Pipelined SAR ADCs

A pipelined SAR ADC shown in Figure 13, a combination of SAR ADCs with a pipelined architecture, can pursue both high energy efficiency as well as high conversion rate. The well-known power burden of opamp needed for the residue amplifier [45]-[47] can be avoided with calibration-assisted open-loop amplifier such as a differential pair with resistor load, a dynamic amplifier, or a gm-cell for current-mode signaling [48]-[55]. The conversion speed of the sub-SAR ADCs can be enhanced by employing the loop-unrolled architecture as in [48]

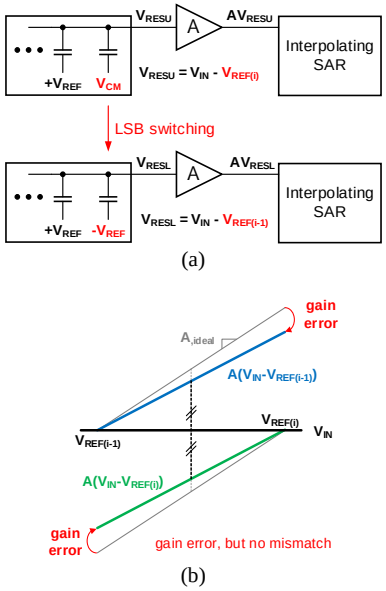

Figure 14. Dual-residue pipelined SAR ADC. (a) CDAC switching for dual residue generation and (b) gain error tolerance of the single-amplifier dual-residue pipelined SAR ADC.

and [52]. [52] could implement a single channel 10b 1.5GS/s ADC in a 14nm FinFET CMOS with only two pipelined stages. One speed limiting factor of a low-power pipelined SAR ADC comes from the limited linearity of open-loop residue amplifiers because we want to have a relatively low voltage residue by increasing the resolution of the coarse SAR ADC. By utilizing linearized input pair for an open-loop amplifier, [54] could reduce the resolution/stage and implemented a single-channel 12b 1GS/s ADC in a 28nm CMOS with three pipelined stages.

Even though open-loop amplifiers can save considerable amount of power consumption compared with opamp-based designs, the mandatory calibration circuitry for the gain and linearity calibration becomes another burden. The dual residue pipelined architecture [56] can eliminate the residue gain accuracy requirement but, instead, requires matched gain between two residue amplifiers. A dual-residue pipelined ADC utilizing only a single residue amplifier can eliminate this matching requirement, and this could be realized by utilizing a SAR ADC as its coarse ADC. It can be implemented by generating two residues sequentially from a single residue amplifier with a 1-LSB CDAC shift as illustrated in Figure 14 [57], [58]. However, the power consumption by the current-mode interpolation in [57] and the parasitic sensitivity of the interpolating CDAC in [58] need further research.

C. Subranging Architectures

The limited conversion speed by the 1b/cycle SA operation can also be improved by taking subranging architecture. In a flash-SAR architecture shown in Figure 15(a), multiple MSBs can be obtained in a single cycle by utilizing a coarse flash ADC, and the

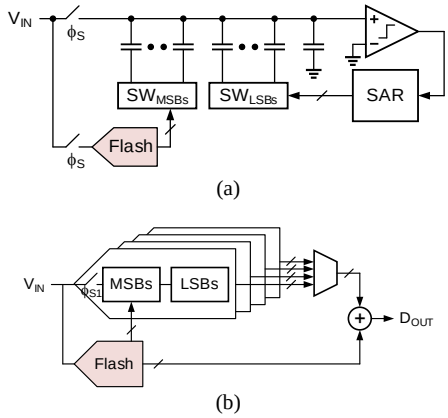

Figure 15. (a) Flash-SAR subranging architecture and (b) time-interleaved flash-SAR architecture.

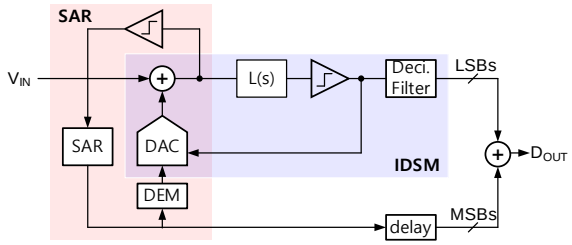

Figure 16. Zoom ADC architecture.

remaining LSBs then can be obtained by the main SAR ADC with remaining small capacitors. This architecture was proved to be efficient for time interleaved SAR ADCs as illustrated in Figure 15(b) because a flash ADC can be fast to be shared by every interleaved sub-SAR ADCs [59]-[61].

A SAR ADC can be also selected for the coarse ADC for speed enhancement purpose even though it is not as fast as a flash ADC: a separate low-resolution coarse SAR ADC can be designed with a much smaller CDAC which can settle much faster than the main ADC with much less switching power. In addition, dumping the obtained MSBs to the main ADC also reduces the switching energy of the main CDAC owing to the small voltage swing on it [18]. On the other hand, sequential transfer of the MSBs can be also used, as in [23], to assign more settling times for the MSBs and thus to hide the capacitor shuffling operation of the main SAR ADC (for improved dynamic linearity).

D. Oversampled SAR ADCs

Combined with oversampling, a SAR ADC could achieve a high SNDR close to 80dB from a 14b SAR ADC [62]. For even higher resolution, nowadays, SAR ADCs are often utilized with noise shaping as in zoom ADCs, noise-coupled delta-sigma modulators (DSMs), and noise-shaping SAR ADCs.

Figure 16 shows the zoom ADC architecture [63] where a SAR ADC is utilized for MSBs decision and the residue is further converted by the following

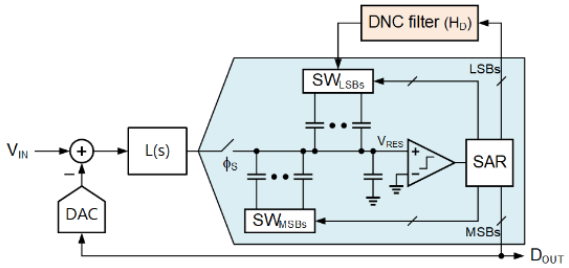

Figure 17. Delta-sigma modulator with digital noise coupling.

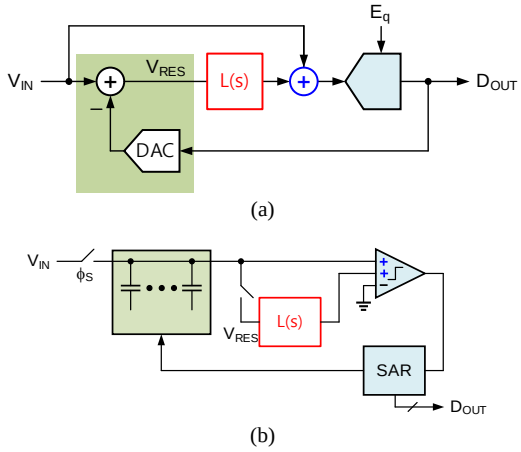

Figure 18. (a) Signal block diagram of NS SAR ADC in the form of CIFF DSM and (b) circuit diagram of NS SAR ADC.

incremental delta-sigma ADC. With dynamic element matching (DEM) for improved dynamic linearity of the SAR DAC, the design in [63] could achieve a 20b resolution with the energy-efficient inverter-based integrator design. Nowadays, the zoom architecture is actively investigated for low bandwidth sensing applications and for audio applications [64], [65].

SAR ADCs can be utilized as a multi-bit quantizer in a DSM. As the CDAC of the SAR ADC can hold the residue after quantization, the residue can be efficiently utilized for further noise shaping in the delta-sigma modulator. In [66], the quantization error after conversion is second-order low-pass filtered and added back to the next input of the quantizer for additional second-order noise shaping. This noise coupling can be simply conducted in digital domain as in [67], as shown in Figure 17. The analog-domain quantization error (residue) remaining on the CDAC (V_{RES}) can be further quantized by resolving more resolution in the SAR quantizer. Then, the digital-domain representation of the quantization error (LSBs) can be filtered in digital domain (DNC filter, H_D) and the digital-filtered residue can be added back to the input of the SAR ADC (in analog domain) by utilizing the LSBs part of the CDAC.

Noise-shaping (NS) SAR ADCs are very popular these days because high resolution can be achieve with low power consumption [68]-[73]. Figure 18(a) shows a conceptual block diagram of the NS SAR ADC.

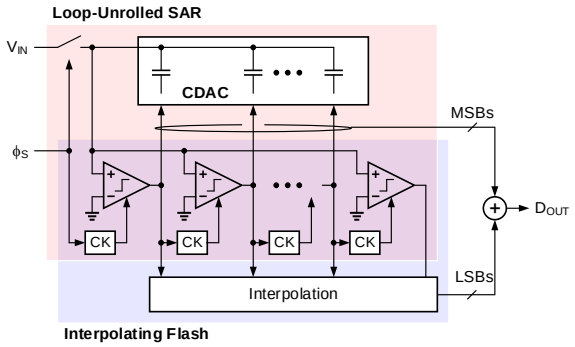

Figure 19. SAR-Flash ADC with shared CDA.

Note that this structure is exactly the same as the cascade-of-integrators-with-feedforward (CIFF) configured delta-sigma modulator, and it is also very similar to that of a SAR ADC when the loop filter noted as L(s) is removed: The path from the input (V_{IN}) to the output of the quantizer which adds a quantization error, E_q, is indeed a SAR ADC itself, and the residue remaining on the CDAC at the end of the entire SAR conversion is V_{RES} (same as E_q). Thus, if we sample the V_{RES} after the SAR A/D conversion is finished and filter it with L(s) and add it with the current input at the input of the comparator, as illustrated in Figure 18(b), this becomes a NS SAR ADC working exactly like a delta-sigma modulator. While an L(s) implemented with an integrator-based filter degrades the low power advantage of the SAR ADC [68], passive-only NS SAR ADCs can preserve low-power advantage with some noise-shaping performance tradeoff [70]-[72]. The limited CDAC linearity of a SAR ADC could be well resolved by DEM for MSBs and the mismatch error shaping for the LSBs, and the design in [69] achieved linearity higher than 100dB. Recently, NS SAR ADC was implemented in a time-interleaved architecture with a proper choice of oversampling ratio and clever usage of decision redundancies, which eliminate the need of complicated mismatch calibration between the time-interleaved ADC channels [73]. The prototype demonstrated a bandwidth of 50MHz and 70.4dB SNDR.

4. EXAMPLE OF A HYBRID SAR ADC

Recently, the authors' group has presented a new high-speed hybrid SAR-Flash ADC architecture [74]. As the simple block diagram in Figure 19 illustrates, a loop-unrolled SAR ADC works as a coarse ADC and the remaining residue on the CDAC is further quantized by the flash ADC. Interestingly, once the usage of the comparators is finished for the loop-unrolled SAR ADC for the MSBs, then, they are reutilized for the flash ADC for the LSBs. In the actual prototype design, four dynamic amplifiers working as preamplifiers for the comparators are shared by a 4b loop-unrolled SAR ADC and a 4.5b backend

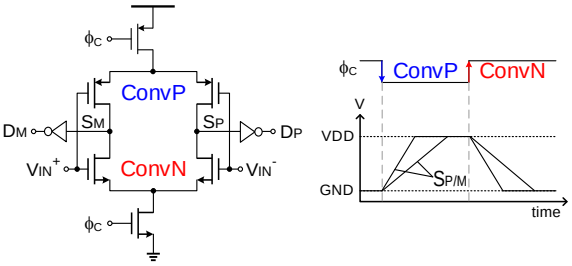

Figure 20. Complementary dynamic amplifier.

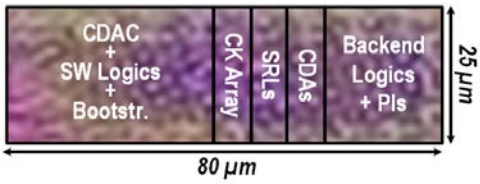

Figure 21. Photo of the ADC core in [74].

Table 1. Performance summary of the ADC in [74]

	This work		ESSCIRC 16' K. Ragab	ESSCIRC 17' G. Wang	VLSI 18' H. Chen	VLSI 18' K. Ohhata
Technology [nm]	28		40	28	40	65
Architecture	LU-SAR + I-Flash, Reused CDAs		LU-SAR	SAR	Two-step SAR	Time-based Subranging
Resolution [bit]	8		8	8	8	8
Supply [V]	1.0	1.1	1.1	0.9	1.2	1.0
f_S [GS/s]	0.9	1.0	0.35	1	1.1	0.95
DNL/INL [LSB]	0.59/0.82		0.9/0.9	<0.5/<0.5	0.58/0.58	0.6/0.8
C_{Hold} [fF]	64		245	79	-	-
Active Area [mm²]	0.002		0.0161	0.00675	0.00165	0.007
$ENOB_{@Nyq.}$ [bit]	7.36	7.26	6.97	6.95	7.18	7.18
Power [mW]	1.88	2.55	1.37	3.2	4.0	2.3
FOM_{Walden} [fJ/c-s]	12.7	16.6	31.3	25.87	25.0	16.7

interpolating flash ADC, in implementing a total of 8b resolution. Considering that an 8b loop-unrolled SAR ADC would require eight comparators and a flash ADC would require even more, this hardware sharing can be a considerable saving. It was possible by the proposed complementary dynamic amplifier (CDA) shown in Figure 20. The PMOS pair of the CDA works for the SAR ADC during ϕ_C is low (ConvP phase) and the NMOS pair works for the flash ADC during ϕ_C is high (ConvN phase). Note that, ideally, the CDA do not need output reset between the two ADC operations because the parking level at the end of one amplification will be the reset level of the next amplification. This reset-free 100% duty operation of the CDA eliminates the energy consumption by the hard reset in a conventional dynamic amplifier. In the actual design, reset switches were utilized to make clear reset with negligible energy consumption. While the PMOS input pair was design for good matching, the NMOS pair was designed asymmetrically in size so that the NMOS pairs can embed decision thresholds for the flash ADC as in [75]. Owing to the small input signal to the flash ADC, the residue of the SAR ADC, the NMOS pairs can work in its linear range and the following multi-stage time-domain interpolation adopted from [76] can resolve further resolution.

A prototype 8b 1GS/s ADC was implemented in a 28-nm CMOS process, and its die photo is shown in

Figure 21. The ADC core size, excluding the CDA offset calibration engine, is as compact as 80 μm × 25 μm owing to the proposed hardware sharing technique. The performance of the prototype ADC is summarized in Table 1. As the CDAC resolution is reduced down to 4b owing to the backend flash ADC, the input capacitance is only 64fF, and this low input capacitance is suitable for a high speed ADC. Under a 1V supply, the ADC achieved an ENOB of 7.36 out of the 8b data and consumes 1.88mW, resulting in a competitive FoM of 12.7 fJ/conversion-step among the ADCs showing similar resolutions and conversion speeds.

5. CONCLUSION

Owing to the digital-friendly simple architecture, SAR ADCs have become the hottest ADC architecture in the nanometer CMOS technology era. Upon the architectural advantage, many advanced circuit techniques and architectures could enhance the cutting-edge performances. The conversion speed could be enhanced with decision redundancy, asynchronous decision, parallel-structured multi-bit/cycle architecture, flash-assisted subranging, and combination with pipelined structure. Small unit capacitors owing to the improved capacitor matching and various CDAC switching techniques could save switching energy. In combination with oversampling and noise shaping technique, SAR ADCs could even achieve very high resolution. One significant contributor that made SAR ADCs to be a major player is the time interleaved architecture and the structure has expanded the spectrum of the SAR ADC applications. However, as the time interleaving technique is more about how to calibrate the mismatches between sub ADCs, they are not discussed in this review. To sum up, SAR ADCs have been proved to be very suitable for nanoscale technologies, and numerous designs have shown that they can remain as a fascinating architecture.

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