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Effect of Channel Variation on Switching Characteristics of LDMOSFET

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ABSTRACT
Electrical characteristics of LDMOS power device with LDD(Lightly Doped Drain) structure is studied with variation of the region of channel and LDD. The channel in LDMOSFET encloses a junction-type source and is believed to be an important parameter for determining the circuit operation of CMOS inverter. Two-dimensional TCAD MEDICI simulation is used to study hot-carrier effect, on-resistance Ron, breakdown voltage, and transient switching characteristic. The voltage-transfer characteristics and on-off switching properties are studied as a function of the channel length and doping levels. The digital logic levels of the output and input voltages are analyzed from the transfer curves and circuit operation. Study indicates that drain current significantly depends on the channel length rather than the LDD region, while the switching transient time is almost independent of the channel length. The high and low logic levels of the input voltage showed a strong dependency on the channel length, while the lateral substrate resistance from a latch-up path in the CMOS inverter was comparable to that of a typical CMOS inverter with a guard ring.

KEY WORDS
LDD, LDMOSFET, CMOS inverter, switching characteristic, latch-up

1. INTRODUCTION

The basic operation of LDMOSFET(lateral double-diffused MOSFET) is similar to that of any other MOSFET. However, the drain-source blocking voltage can be in the range of a few tens volt and the current driving capability of this device is usually high. The advantages of LDMOSFET are that it requires only a small input current [1-3]. Moreover, the high switching speed can be controlled with a very small gate current.

LDMOSFET power device is in great demand in RF power amplifier and power switching device [4-8]. While the scaling down of the power device shows a few important advantages in terms of power consumption and switching time, the decrease can cause a significant change of other power characteristics [9-13]. which are the switching resistance, breakdown voltage, and SOA(safe operating area) region. In order to increase the breakdown voltage, the carrier depletion region seems to be larger. The drift region is to be increased and the doping concentration can be another unknown element. The maximum allowed current density is also supposed to significantly dependent on the drift region and doping concentration. In this paper, electrical characteristic of LDMOSFET is studied with variation of impurity concentration and length in the region of channel and drift. Device simulation is carried out with MEDICI simulator to study I-V characteristics, change of ON-resistance, and OFF transient characteristics.

2. RESULT

LDD MOSFET is largely divided in the three regions of channel region, drift region, and npn BJT region as shown in Figure 1. As the drift region in the figure is lightly doped, the scaling down of device and high drain voltage does not produce a hot carrier degradation and problem of device reliability problem. Compared to IGBT and VDMOS, LDMOS is known to be better in latch-up characteristics.

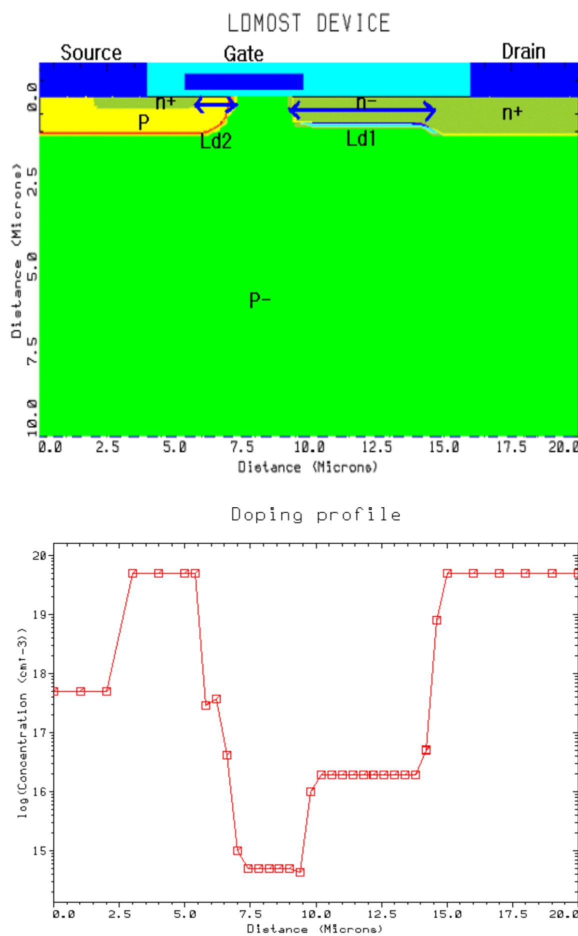

Figure 1. Cross-section and doping profile of LDMOSFET.

The equi-potential and electric field line in the cross-section of this device are shown in Figure 2. The equi-potential lines concentrate on the edge of gate, which means relatively high electric field in the LDD region. With increase of drain voltage, the depletion region of junction increases and the effective area of current flow becomes smaller, therefore, the drain current can be constant as the carriers have a saturated drift velocity near drain.

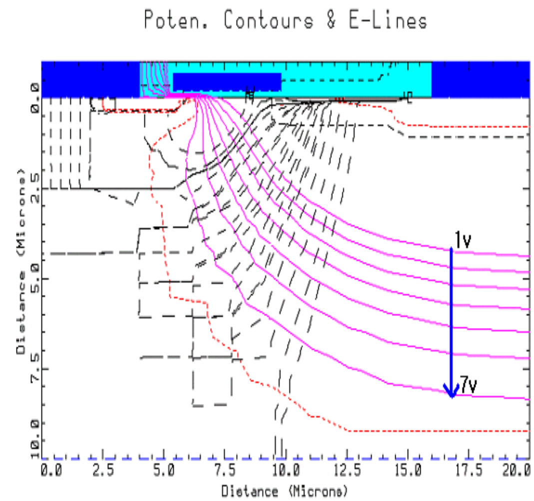

Figure 2. Equipotential and electrical field lines of cross-section of LDMOSFET.

The characteristics of drain voltage and current with change of the length of drift region(the length of LDD) is shown in Figure 3. We have noticed that the drain current changes relatively small within 5% and the resistance under 5V drain voltage(Ron) is almost constant with change of the LDD length.

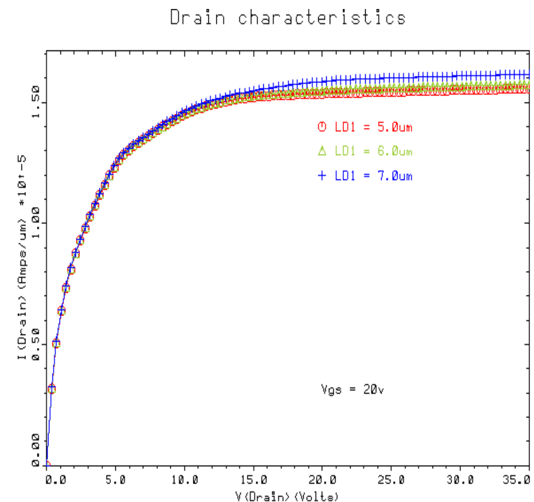

Figure 3. I-V characteristics with variation of the drift length(Ld1).

Similarly to Figure 3 and Figure 4. explains the characteristics of drain voltage and current with change of impurity concentration at the constant LDD length. The drain current increases with increase of impurity concentration. The electron current which is a majority carrier in LDD region is known to be the drift current and be proportional to the multiple of an impurity concentration. The drain current is expected to increase, while the breakdown voltage decreases inversely.

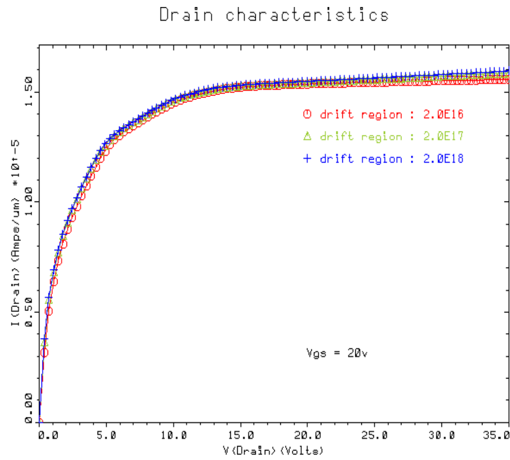

Figure 4. I-V characteristics with variation of impurity concentration in the drift region.

In order to see the effect of the channel length(Ld2), the characteristics of drain current versus drain voltage and gate voltage is shown in Figure 5 and Figure 6. In Figure 5 the saturated drain current in the active area is shown to be increased with decrease of the channel length and the ON resistance is increased with increase of the channel length(Ld2). In the Figure 6 which shows the drain current versus the gate voltage at constant drain voltage, the conductance decreases with increase of the channel length(Ld2), which can be come from the fact that a resistance is proportional to the length of current flow.

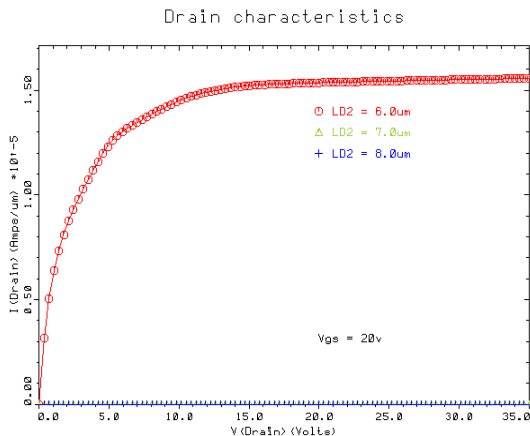

Figure 5. I-V characteristics with variation of the channel length(Ld2).

The conventional CMOS inverter is the most popular digital logic circuit because of low power dissipation and high speed[3,4]. Currently, a typical CMOS inverter does not meet the needs for diverse power applications in a digital circuit. A new type of CMOS inverter for a wide power supply range and a large output voltage swing in a digital driver IC was suggested.

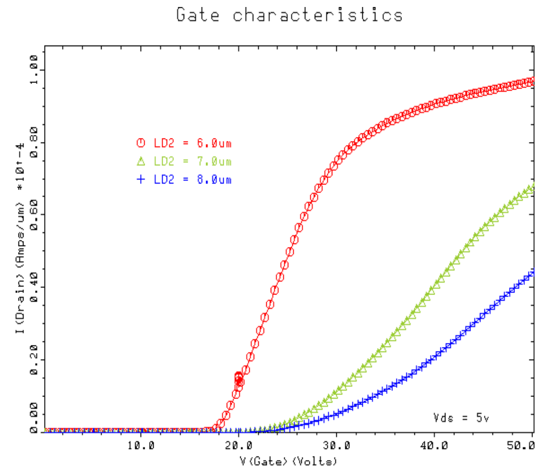

Figure 6. Characteristics of drain current versus gate voltage with variation of the channel length.

A LDMOSFET pair in CMOS inverter was examined for a high power application and high speed. Compared with a typical CMOS inverter, a LDMOSFET complementary inverter is believed to have good latch-up immunity and high voltage allowance due to the p/n junction-type source. The junction-type source in LDMOSFET can control the channel parameters to provide a high voltage swing in digital logic, and eliminate the need for a guard ring for latch-up immunity in a CMOS inverter, which is the most effective way of preventing latch-up.

The electrical characteristics of a LDMOSFET CMOS inverter were examined in terms of the voltage transfer characteristics, on-off switching properties and latch-up with a variation in the n-channel length and impurity concentration. Figure 7 shows a cross section of the CMOS inverter, where LDMOSFET has the typical structure consisting of a drift region and a main channel enclosing the source region. With the output node constrained to swing from ground to V_{DD}, the drain-to-body junctions in the n-channel device are always reversed-biased. A simulation is carried out using a TCAD MEDICI simulator.

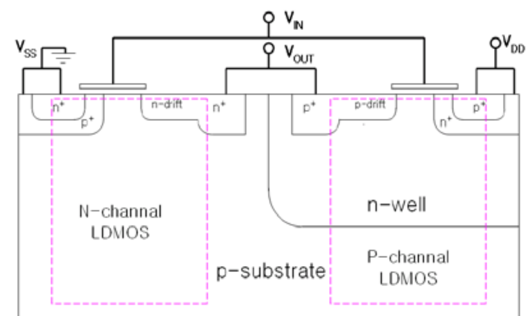

Figure 7. Cross section of a CMOS inverter using LDMOSFET.

Figure 8 shows the voltage transfer characteristic of a CMOS inverter, where A, B, and C correspond to the 3 different channel lengths of 0.5 μm, 1.0 μm, 1.5 μm, respectively. The voltage transfer characteristics were obtained by varying the n-channel length at a doping level of 5E16 cm^{-3}. Each transfer characteristic has five distinct segments corresponding to the different modes of operation of the p and n-channel LDMOSFET. The first segment of the transfer characteristics was obtained when the p-LDMOSFET was in the triode region and the n-LDMOSFET was under saturation conditions, while the last segment is in an opposite operating region. The other segments were the interface regions and uncertainty region. The two cases of logic input voltages were considered: low input voltage V_{IL} when the input voltage, V_I, is at the logic-0 level; and the high input voltage, V_{IH}, when the input voltage, V_I, is at the logic-1 level.

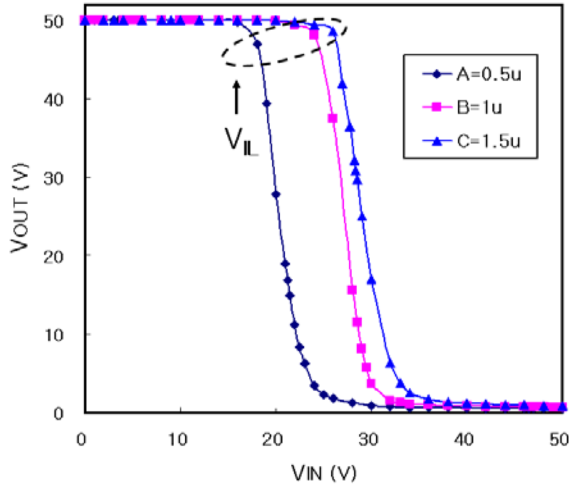

Figure 8. Voltage transfer characteristic of a CMOS inverter as a function of the n-channel length.

V_{IL} increased with increasing n-channel length. The result arises from the dependency of the threshold voltage and the conductance of the LDMOSFET on the channel length. The high and low digital output logic levels were almost in the output voltage where the input voltages V_{IL} and V_{IH} are located. The logic output voltages did not show as strong a dependency on the channel length as the input voltages of V_{IL} and V_{IH}. The effect of the n-channel length on the output logic levels can be observed in the equipotential lines at a gate voltage of approximately 25 V, as shown in Figure 9. It indicates that the p-channel LDMOSFET is in the higher potential compared with the n-channel one. The output current flows between the n-channel MOS and V_{SS}. Consequently, the output voltage is at the logic-0 level.

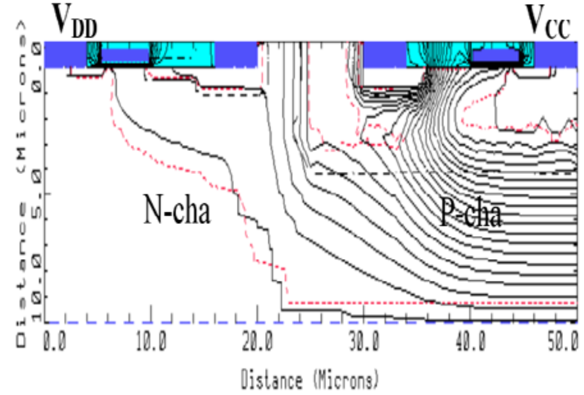

Figure 9. Cross-sectional view of the equipotential lines at a 0.5 μm channel length with Vg=25 V.

Figure 10 shows the I_D-V_{DS} (Drain current versus voltage) curve for the n-channel LDMOSFET Q_N, when V_I = V_{DD}. In Fig. 10, the n-channel LDMOSFET is considered to be the driving transistor, and the p-channel LDMOSFET is considered to be the load.

When the input is high(V_{DD}), the n-channel device is turned on, the p-channel device is off. Hence, there is no dc path from V_{DD} to V_{SS}. The load curve is superimposed on the curves of the n-channel device. Since the p-channel device Q_P is turned off, the load curve will be at almost a zero current level. The current-voltage curves of the driver were obtained as a function of the n-channel length.

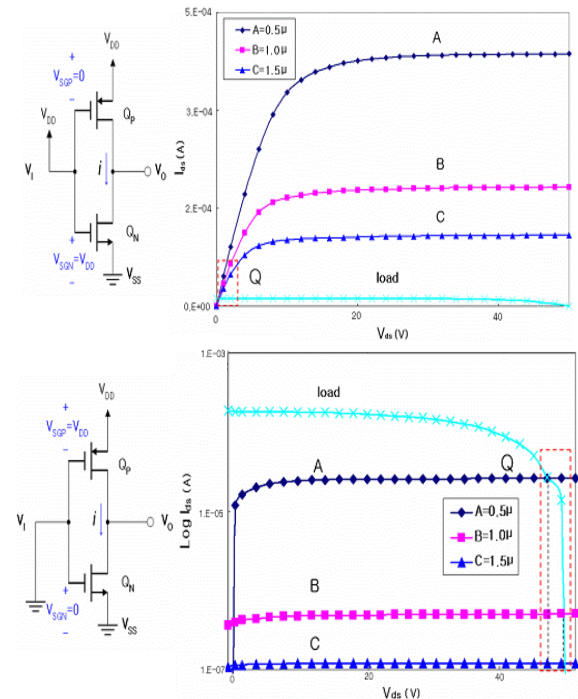

Figure 10. Operation of the CMOS inverter as a function of the channel length when the input voltage VI is high.

The operating point will be at the intersection of the two curves, where the output voltage is almost zero, and the output voltages are almost same regardless of the channel length. An analysis of Figure 10 indicates that the n-channel length does not affect on the output logic levels of V_{OH} and V_{OL}.

Figure 11 and Figure 12 show the transient characteristics of the drain current in the OFF state, which indicates the transient time is almost independent of the change of LDD length (Figure 11) and channel length (Figure 12). This result verifies the fast switching property of MOSFET which is almost independent of the device structure. The dependence of breakdown voltage on the channel length is shown in Figure 13. The breakdown voltage is the voltage where the drain current is abruptly increased. The figure indicates that the breakdown voltage is increased with increase of channel length. But, we found in other study that the length of drift region does not effect on the breakdown voltage.

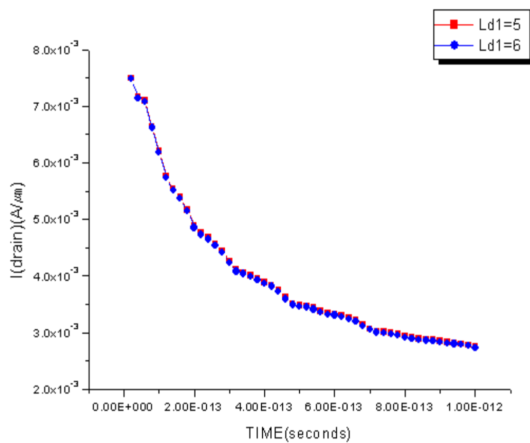

Figure 11. Transient characteristics in the OFF-state with two different drift length.

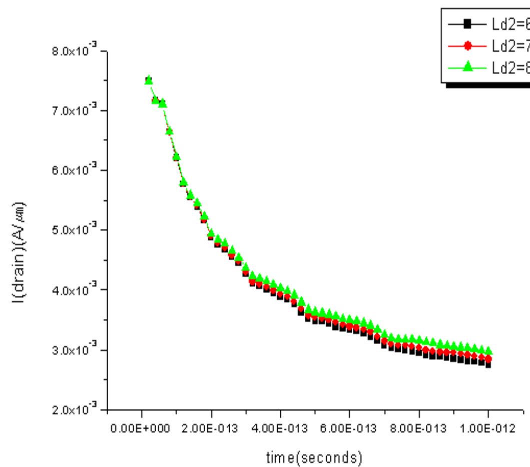

Figure 12. Transient Characteristics in the OFF-state with variation of the channel length.

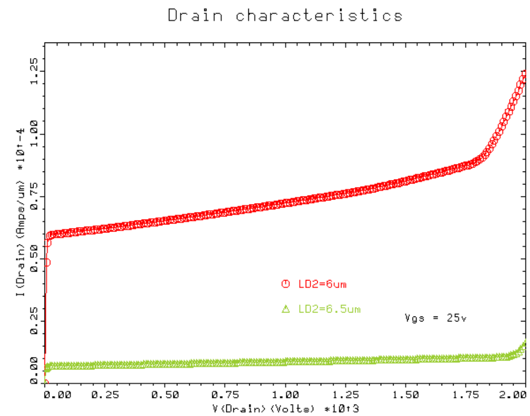

Figure 13. Comparison of breakdown voltages with two different channel length.

The CMOS circuit is susceptible to latch-up due to of the presence of a pnpn structure. The four-layer structure of the n-well process arises from a p^+ source, n-well, a p substrate, and an n^+ drain. The layout technique and process change are effective ways of preventing latch-up. The CMOS inverter using LDMOSFET is considered to have a structure of latch-up immunity by reducing the substrate and well resistance.

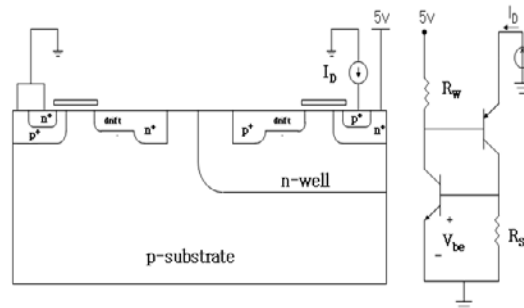

Figure 14. Circuit of the latch-up path for the measurement of the substrate resistance, Rs.

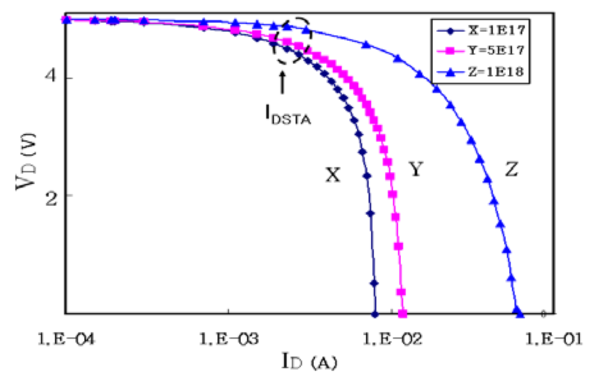

Figure 15. I-V characteristics for the Rs measurement as a function of the n-channel doping levels.

Figure 14 shows a cross-sectional view and circuit of the latch-up path for measuring the substrate

resistance (Rs). The p/n junction-type source is considered to decrease the substrate resistance(Rs) and well resistance (Rw). With increasing current from the current source, which is connected to an emitter of a parasitic npn transistor, the emitter-base voltage(V_D) maintains a 5 V saturation state. At the moment of the turn-on state of the parasitic npn transistor, the voltage, V_D, decreases drastically. From this, the triggering current, Is, can be obtained. The substrate resistance, Rs, was measured from the triggering current, Is, and a saturation voltage of 0.6 V between the base and emitter in the pnp transistor. In Figure 15, the substrate resistance(Rs), which was obtained when the voltage, V_D, decreases drastically, decreases with increasing channel doping. The measured substrate resistance(Rs) is in the 1 ㏀ range, which is almost the same range in a typical CMOS inverter with a guard ring. Display driver circuit usually consists of a level-shifter and CMOS inverters. In order to reduce the latch-up problem, the optimum circuit design comes along with substrate resistance (Rs) of CMOS inverter.

3. CONCLUSION

Electrical characteristics of LDMOSFET power device is studied with variation of the length of channel and LDD region, and impurity concentration. In the 2-D MEDICI simulation, the impurity concentration and the length in LDD region provide a negligible effect on Ron and drain current, while the channel length effects on the DC characteristics. The drain current decreases with increase of the channel length, while the on-resistance is linearly proportional to the channel length. The transient characteristic in the off-state is found to be almost independent of the LDD length (Ld1). The electrical characteristics of a LDMOSFET CMOS inverter are also investigated as a function of the channel length and impurity concentration. The transfer characteristics of the CMOS inverter and the on-off switching operation showed a strong dependency on the channel length. The digital logic levels of the input voltage increased with increasing n-channel length, while those of the output voltage showed no dependency. The junction-type source decreased the lateral substrate resistance resulting in good latch-up immunity. Consequently, the study of channel region in LDMOSFET is supposed to be an effective method to improve the electrical characteristics of CMOS inverter as well as it's switching property.

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REFERENCES

[1] N. Fjjishima, Akio Sugi, Satomi Kajiwara, Kunio Matsubara, Yoshihiko Nagayasu, and C. Andre T. Salama, "A high density, low on-resistance, trench lateral power MOSFET with a trench bottom source contact", Proc. ISPSD, p.143, 2001.

[2] T. Kubota, Kiminori Watanabe, Kumiko Karouji, Mitsuru Ueno, Yasuko Anai, Yusuke Kawaguchi, and Akio Nakagawa, "Cost-effective approach in LDMOS with partial 0.35 ㎛ design into conventional 0.6 ㎛ process", Proc. ISPSD, p. 245, 2003.

[3] M. G. Johnson, "A symmetric CMOS NOR gate for high speed application", IEEE JSSC, Vol. Sc-23, No. 5, p. 1233, 1988.

[4] C. S. Lee, Y. J. Oh, K. Y. Na, Y. S. Kim, and N. S. Kim, "Integrated BiCMOS control circuits for high-performance DC-DC boost converter," IEEE Trans. Power Electronics, vol. 28, no. 5, pp. 2596-2603, May 2013.

[5] H. Kim, S. Ahn, and N. Kim, "CMOS integrated time-mode temperature sensor for self-refresh control in DRAM memory cell," IEEE Sensors Journal, vol. 16, no. 17, pp. 6687-6693, 2016.

[6] Sung-Wan Hong, Sang-hui Park, Tae-Hwang Kong, and Gyu-Hyeong Cho, "Inverting buck-boost DC-DC converter for mobile AMOLED display using real-time self-tuned minimum power-loss tracking (MPLT) Scheme with Lossless Soft-Switching for Discontinuous Conduction Mode," IEEE J. of Solid-state Circuits, vol. 50, pp. 2380–2393, 2015.

[7] Na K. Y., Ha J. B., Choi M. H., Kim N. S., and Kim Y. S., "Optimizing the gate-to-drift overlap length of lateral double diffused metal-oxide-semiconductor field effect transistor devices to improve hot-carrier device lifetime", Japanese Journal of Applied Physics, Vol. 45, No. 3A, p.1525, 2006.

[8] J. scholvin, J. G. Fiorenza, and J. A. del Alamo, "The impact of substrate surface potential on the performance of RF power LDMOSFETs on high–resistivity SOI", IEDM, Tech. Dig., p. 363, 2003.

[9] P. H. Wilson, "A novel trench gate LDMOS for RF applications", Microwave and Telecommunication Technology, 2003.CriMiCo 2003. 13th internation-al Crimean conference, p. 214, 2003.

[10] Marn-Go Kim, "Error amplifier design of peak current controlled (PCC) buck LED driver," IEEE Trans. Power Electronics, vol. 29, no. 12, pp. 6789-6795, 2014.

[11] H. Du, X. Lai, C. Liu, and Y. Chi, "Low quiescent current linear regulator using combination structure of bandgap and error amplifier," Electronics letters, vol. 50, no. 10, pp. 771-773, 2014.

[12] S. Ikeda, S. Yeop, H. Ito, N. Ishihara, and K. Masu, "A 0.5 V 5.96-GHz PLL with amplitude-regulated current-reuse VCO," IEEE Microwave and Wireless Components Letters, vol. 27, issue 3, pp. 302-304, 2017.

[13] P. Liu, T. Chen, and S. Hsu, "Area-efficient error amplifier with current-boosting module for fast-transient buck converters," IET Power Electronics, vol. 9, iss. 10, pp. 2147-2153, 2016.

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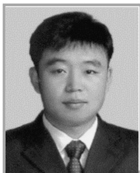

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